

## GaAs MMIC Low Noise Amplifier Chip, 0.01-3.5GHz

### Performance characteristics

- Frequency range: 0.01-3.5GHz
- Small signal gain: 30.5dB
- Noise figure: 0.75dB Typ.
- P-1dB: 18dBm
- Power supply: +5V/70mA
- Input/Output: 50Ohm
- 100% on-chip testing
- Chip size: 1.25 x 1.25 x 0.1 mm

### Product Introduction

GLA-0003B is a broadband low noise amplifier chip with a frequency range of 0.01GHz~3.5GHz, small signal gain of 30.5dB and in-band noise factor of 0.75dB. The GLA-0003B is powered by a single +5V power supply.

#### Use restriction parameters<sup>1</sup>

Maximum leakage voltage	+7V
Maximum input power	+20dBm
Working temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of the above maximum limits may result in permanent damage.

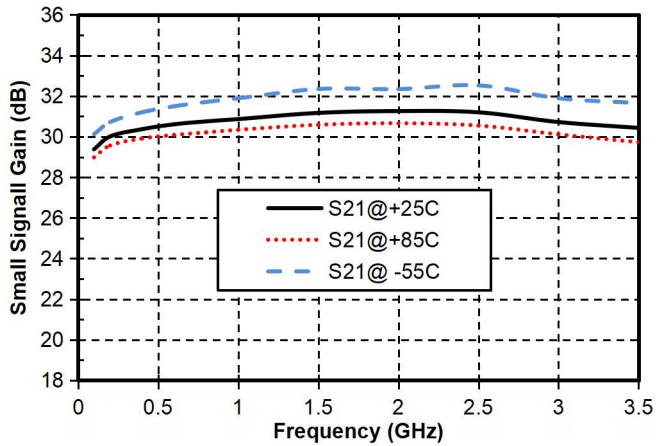
#### Electrical performance parameters( $T_A = +25^\circ\text{C}$ , $V_d = +5\text{V}$ , $R = 8\Omega$ )

Index	Minimum value	Typical value	Maximum value	Unit
Frequency range	0.01-3.5			GHz
Small signal gain	29	30.5	-	dB
Gain flatness	-	$\pm 0.5$	-	dB
Noise figure	-	0.6	-	dB
P-1dB	-	18	-	dBm
Psat	-	19	-	dBm
Input return loss	10	15	-	dB
Output return Loss	14	18	-	dB
Static current	70			mA

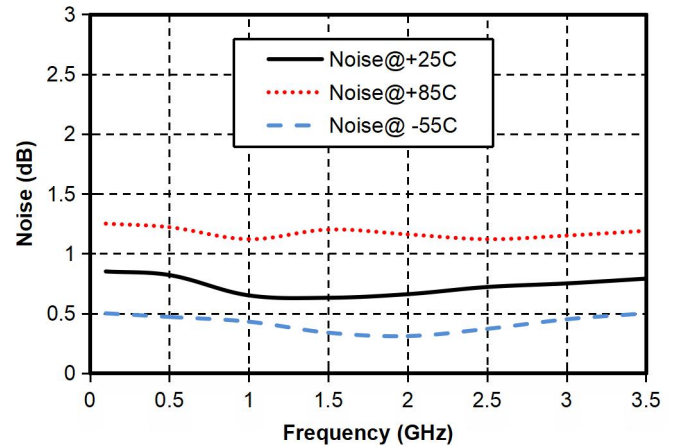
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Main indicator testing curve

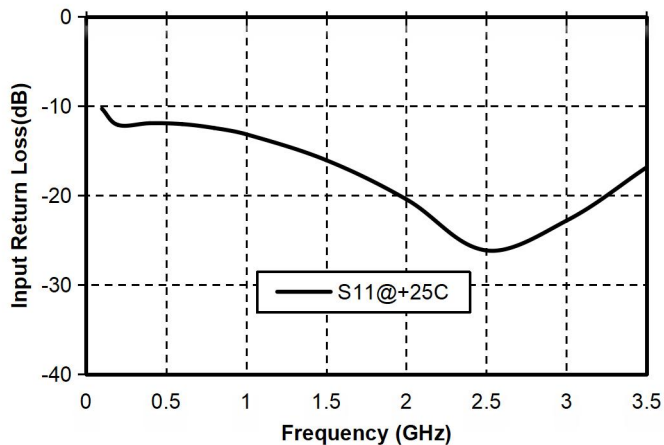
Gain vs. Frequency range



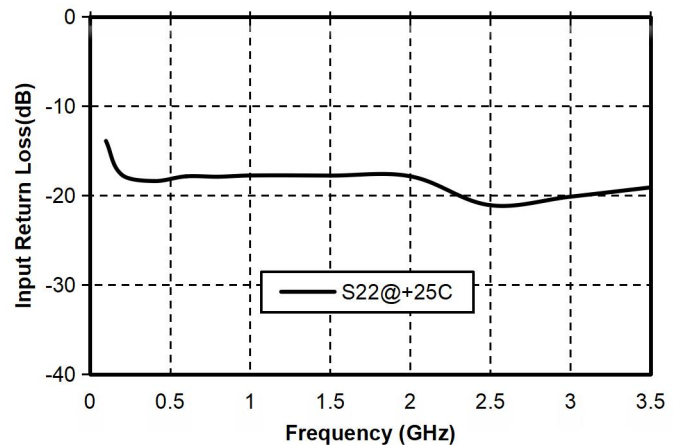
Noise Figure vs. Frequency



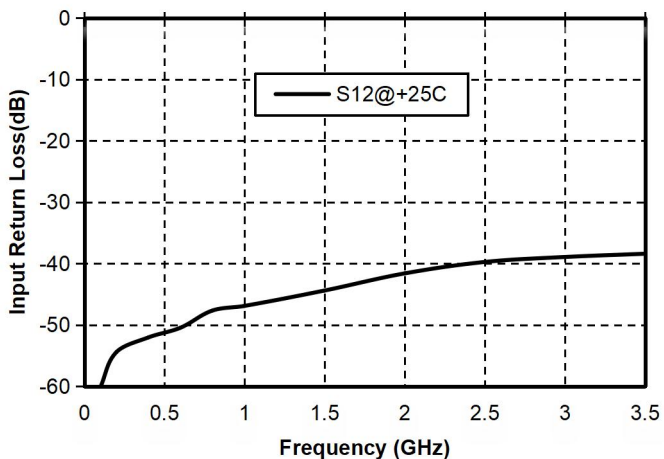
Input return loss vs. Frequency



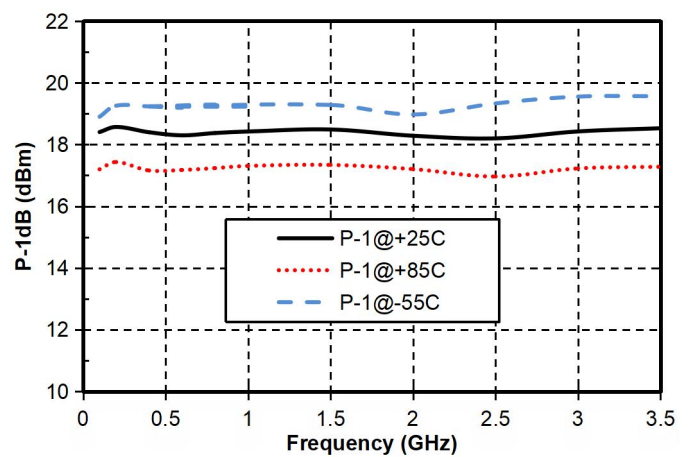
Output return Loss vs. Frequency



Reverse isolation vs. Frequency

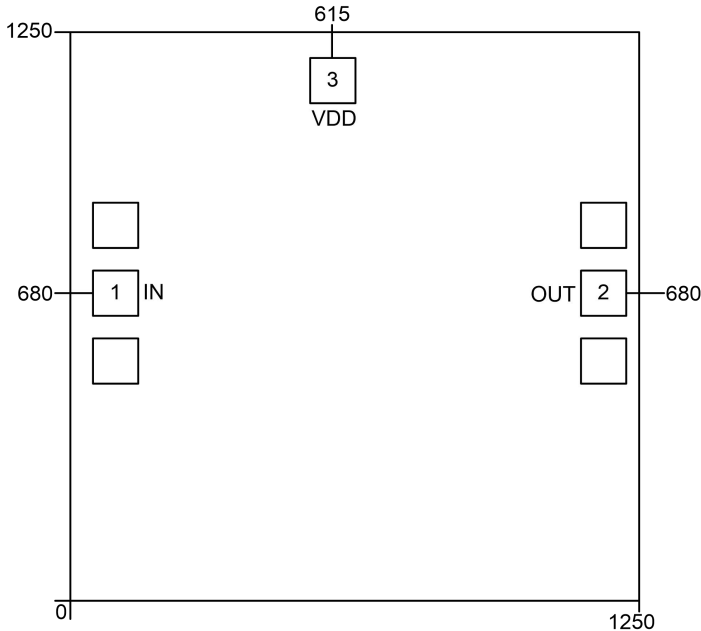


P-1dB vs. Frequency



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### External structure<sup>2</sup>

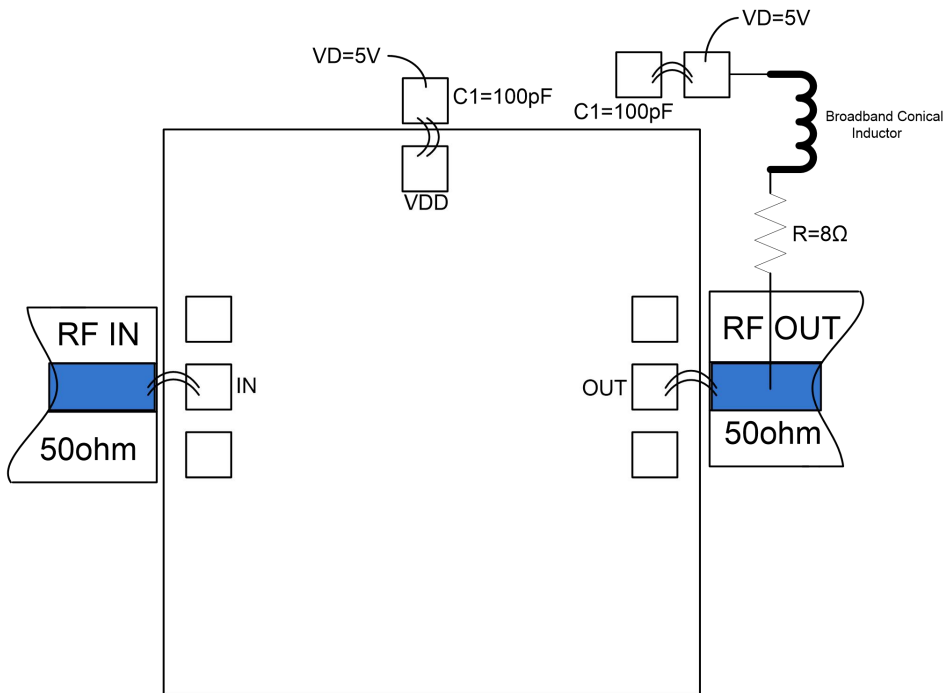


【2】 The units in the figure are all millimeters, with a tolerance of  $\pm 100\mu\text{m}$ .

Definition of bonding pressure point		
Bond point number	Functional symbols	Function Description
1	RFIN	RF signal input terminal requires the installation of a DC isolation capacitor.
2	RFOUT、VDD	The RF signal output terminal needs to be equipped with a DC isolation capacitor; Amplifier drain bias; External 100pF bypass capacitor required, external $8\ \Omega$ resistor and 56nH~220nH choke inductor required.
3	VDD	Amplifier drain bias; External 100pF bypass capacitor required.
Chip bottom	GND	The bottom of the chip needs to be well grounded with RF and DC.

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### Recommended assembly diagram



### Notice

- The chip needs to be stored in a container with anti-static function and stored in a nitrogen environment.
- Attempting to clean the surface of bare chips using wet chemical methods is prohibited.
- Please strictly comply with ESD protection requirements to avoid static damage to bare chips.
- Routine operation: Please use precision pointed tweezers to remove the bare chip. During the operation, avoid tools or fingers touching the surface of the chip.
- Suggestion for mounting operation: Bare chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold tin ratio of 80/20. The working surface temperature reached 255 °C, and the tool (vacuum chuck) temperature reached 265 °C. When a high-temperature mixed gas (nitrogen to hydrogen ratio of 90/10) is blown onto the chip, the temperature at the top of the tool should be raised to 290 °C. Do not let the chip stay above 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive adhesive applied should be as small as possible. After placing the chip in the installation position, the conductive adhesive can be vaguely visible around it. Please follow the information provided by the conductive adhesive manufacturer for curing conditions.
- Suggestion for bonding operation: Both spherical or wedge-shaped bonding should be used  $\Phi$  0.025mm (1mil) gold wire. Thermal ultrasonic bonding temperature is 150 °C. The pressure of the

spherical bonding cutter is 40-50GF, and the pressure of the wedge bonding cutter is 18-22GF. Use as little ultrasonic energy as possible. The bonding process starts at the pressing point on the chip and ends at the packaging (or substrate).