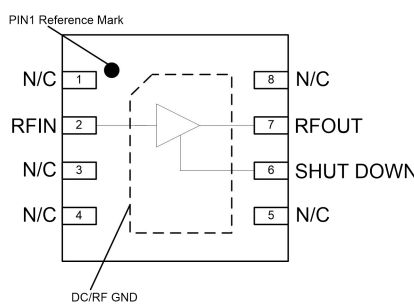


High Linearity Low Noise Gain Amplifier , 200 - 6000MHz

Product Introduction

GHLN-90 37-DF2-8 is a 200MHz ~ 6000MHz ultra - wideband, high linearity, low noise gain block amplifier. This amplifier can meet the needs of a variety of application scenarios, including small base stations, walkie-talkies, LTE/WCDMA communication systems and other wireless communication systems. GHLN-90 37-DF2-8 adopts the standard DFN2X2 label package. The amplifier integrates shutdown bias capability and all pins are equipped with ESD protection. The product quality level is industrial grade.

Block Diagram	Product Features
 <p style="text-align: center;">Bottom view</p>	<p>Working frequency band : 200-6000MHz Noise figure: 0.4dB@1950MHz Small signal gain: 21dB @ 1900 MHz P-1dB: 20.5dBm OIP3: 35 dBm Integrated shutdown function 50Ohm input and output +5V /70mA 2x2 mm 8 Pin DFN plastic package</p>

Electrical performance parameters (TA = +25°C, Vd = +5V, 50Ω system)

Index	Test Conditions	Minimum	Typical Value	Maximum	Unit
Frequency Range		50		6000	MHz
Test frequency			1950		MHz
Small Signal Gain			21		dB
Input return loss			12.5		dB
Output return loss			11.5		dB
P-1			20.5		dBm
OIP3	Pout=+ 5 dBm/tone, Δf =1 MHz		35		dBm
Noise Figure*	Without de-embedding, the estimated evaluation board loss is 0.15dB@1.9G		0.55		dB
Switching speed	Rise Time (10%-90%)		120		ns
	Fall Time (90%-10%)		350		ns
Shutdown control	On state	0		0.4	V
	Off state (Power down)	+ 2.5	+ 3.3	VDD	V
Current	On state		70		mA
	Off state (Power down)		140		uA
Shutdown pin current	VPD ≥ 2.5 V		250		uA
Thermal resistance	channel to case			60	°C/W

*The noise figure result does not deduct the input loss of the test DEMO board .

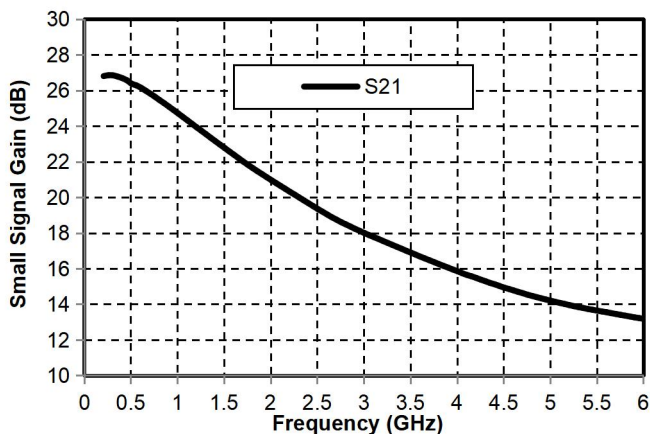
High Linearity Low Noise Gain Amplifier , 200 - 6000MHz

200M-6000M electrical performance parameters:

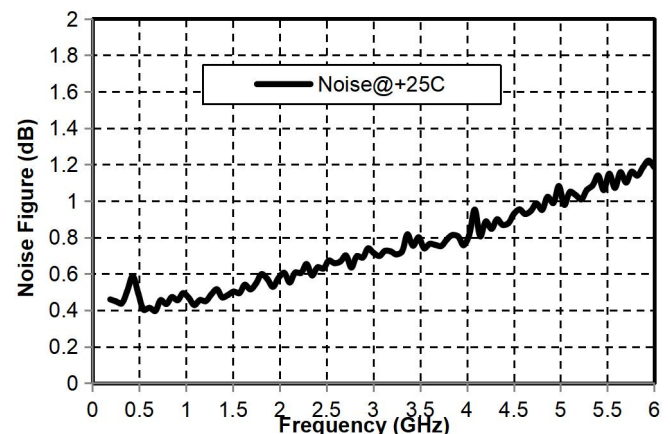
Electrical performance parameters (TA = +25°C, Vd = +5V, Ids = 70mA, 50Ω system)							
Index	Test Conditions	Typical Value					Unit
Test frequency		200	900	1700	2300	5000	MHz
Small Signal Gain		26.5	25	22	20	14	dB
Input return loss		5	10	12	13	11	dB
Output return loss		9.5	14	12	11	9.5	dB
P-1		19	20	20.5	20	20	dBm
OIP3	Pout=+ 5 dBm/tone, Δf =1 MHz	35	36	35	34.5	33.5	dBm
Noise Figure*		0.5	0.5	0.5	0.6	1.0	dB

*The noise figure result does not deduct the input loss of the test DEMO board .

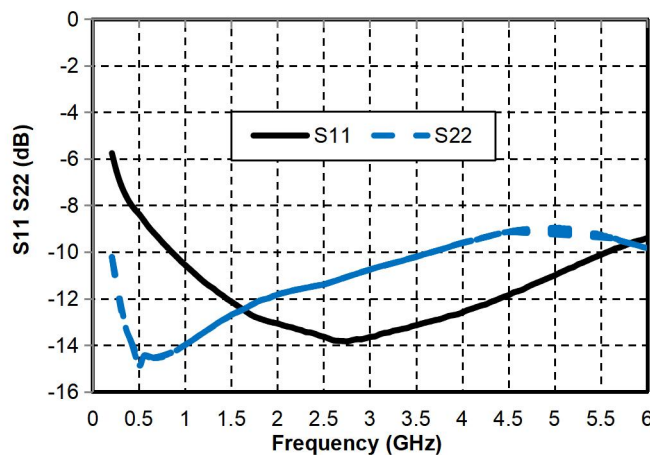
Main index test curve (TA = +25°C , Vcc = + 5V)



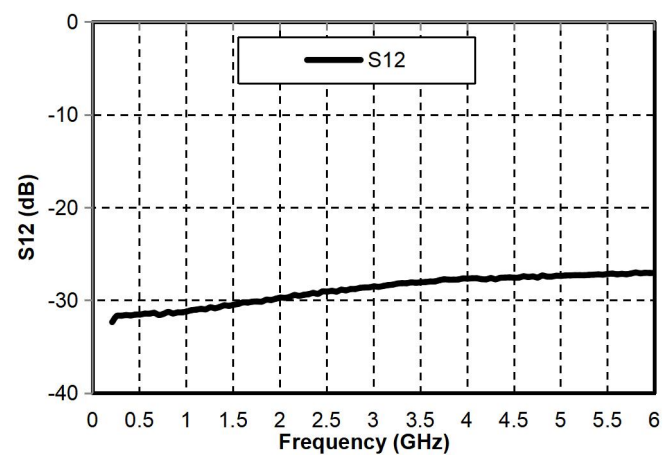
Small Signal Gain vs. Frequency



Noise Figure vs. Frequency

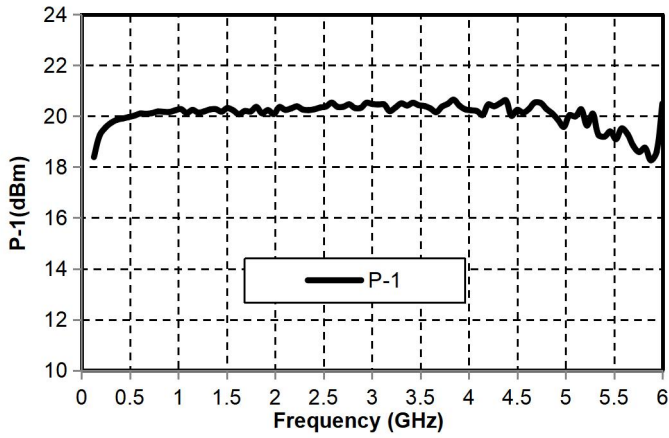


Input /Output Return Loss vs. Frequency

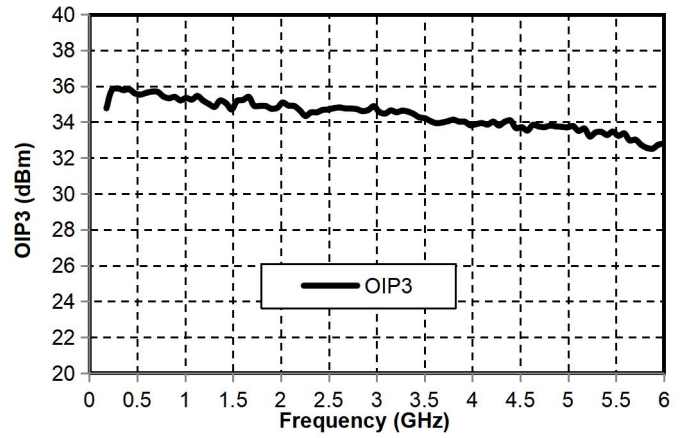


Reverse Isolation vs. Frequency

High Linearity, Low Noise Gain Block Chip, 0.02 - 6 GHz



P-1dB vs. Frequency



OIP3 vs. Frequency

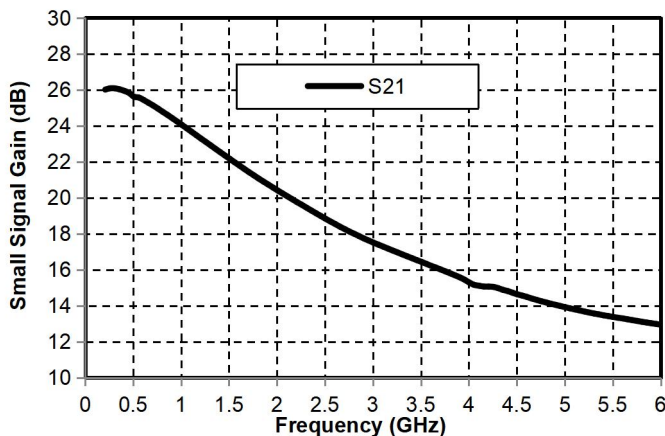
High Linearity, Low Noise Gain Block Chip, 0.02 - 6 GHz

200M-6000M electrical performance parameters

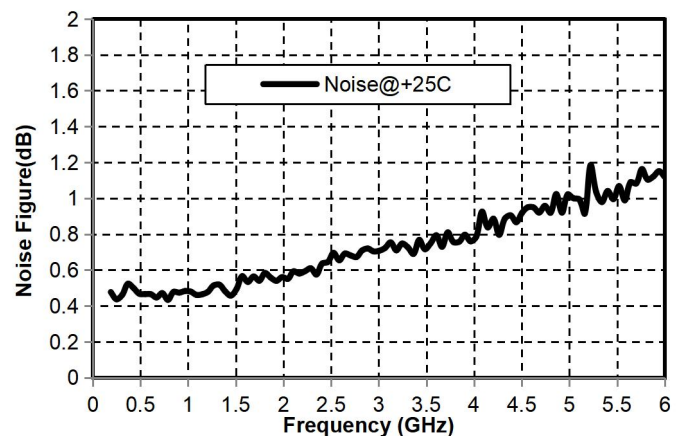
Electrical performance parameters (TA = +25°C, Vd = +3.3V, Ids = 45mA, 50Ω system)							
Index	Test Conditions	Typical Value					Unit
Test frequency		200	900	1700	2300	5000	MHz
Small Signal Gain		26	24	21	19	14	dB
Input return loss		5	8	10	11	10	dB
Output return loss		10	14	12	11	9	dB
P-1		16	17	17.5	17.5	17	dBm
OIP3	Pout=+ 2 dBm/tone, Δf =1 MHz	30	31.5	32	32.5	33.5	dBm
Noise Figure*		0.5	0.5	0.5	0.6	1.0	dB

*The noise figure result does not deduct the input loss of the test DEMO board .

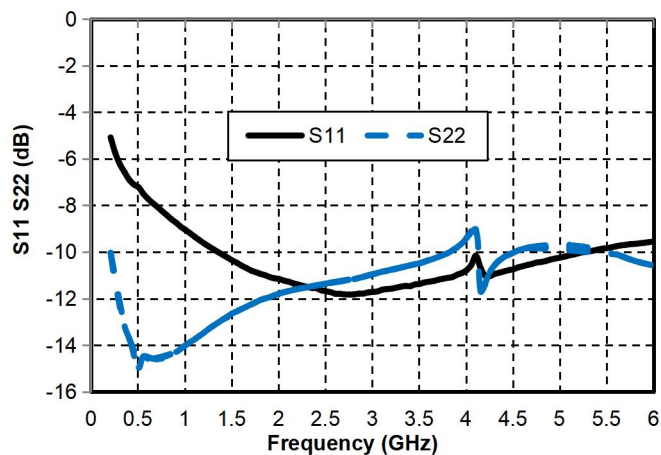
Main performance test curve (TA = +25°C , Vcc = + 3.3V)



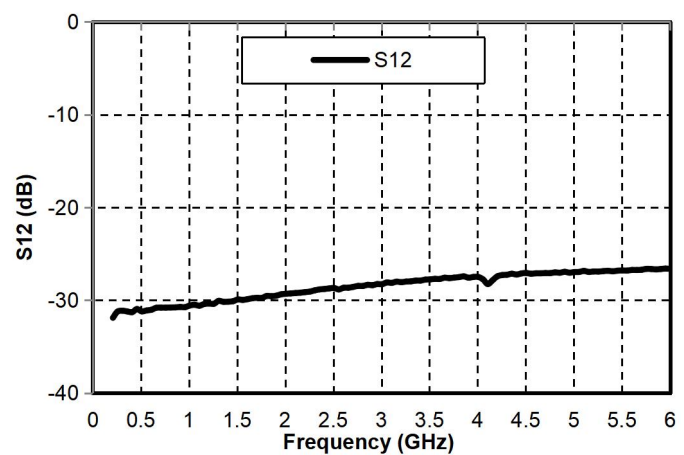
Small Signal Gain vs. Frequency



Noise Figure vs. Frequency

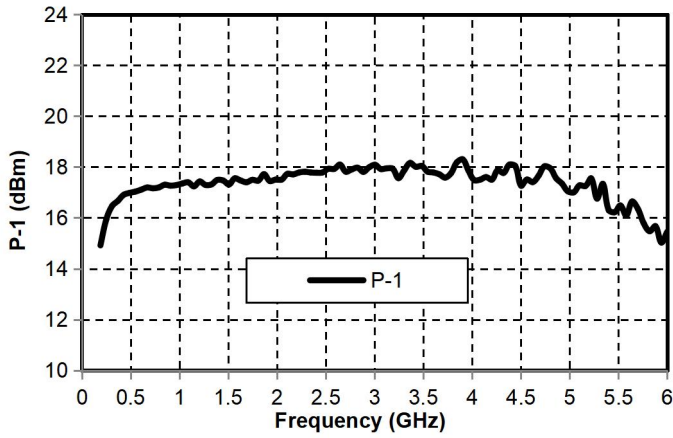


Input /Output Return Loss vs. Frequency

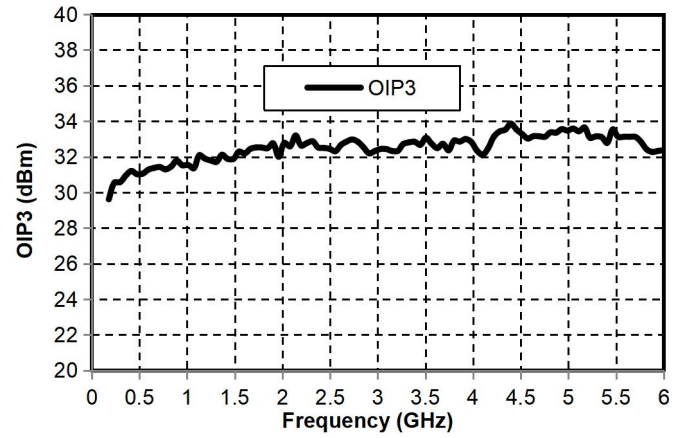


Reverse Isolation vs. Frequency

High Linearity, Low Noise Gain Block Chip, 0.02 - 6 GHz



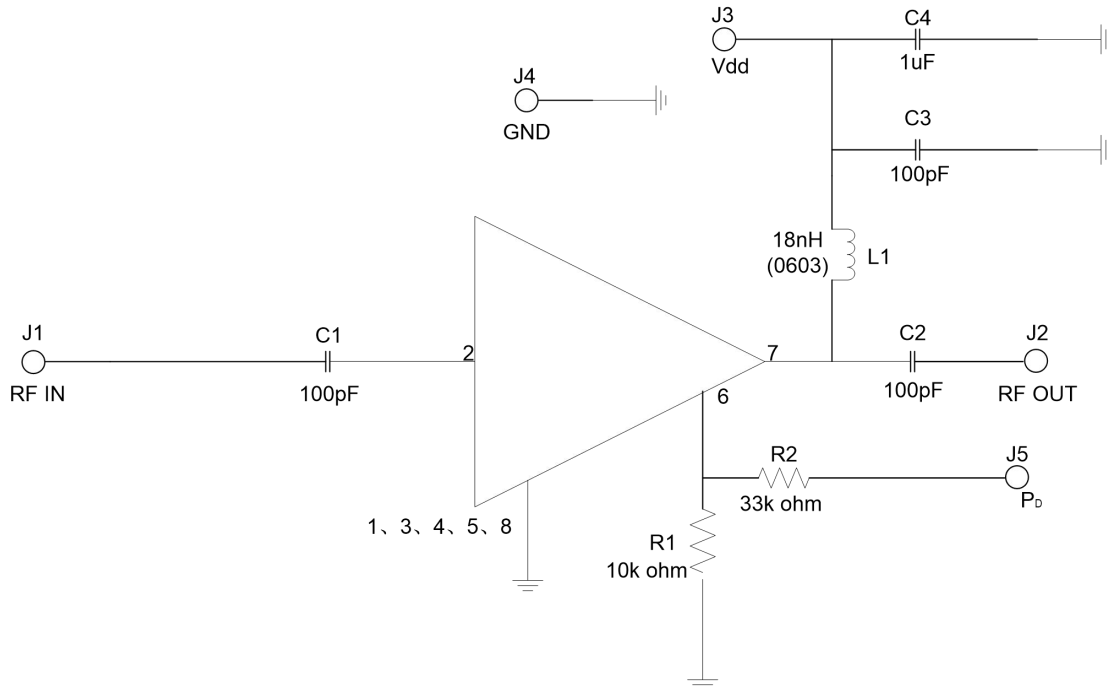
P-1dB vs. Frequency



OIP3 vs. Frequency

High Linearity, Low Noise Gain Block Chip, 0.02 - 6 GHz

200M-6000M recommended circuit diagram



Precautions

- 1、 All resistors and capacitors are packaged in 0402
- 2、 The capacitance values of C1 , C2 and C3 need to be adjusted according to the actual application frequency.
- 3、 The inductance values of L1 and L10 need to be adjusted accordingly according to the actual application frequency.
- 4、 If not needed, R2 can be not installed; when R2 is not installed, the amplifier is always in working condition.

Ingredients list

Raw material	RC Inductance	Describe	Brand
R 1	10kΩ	Resistor, Chip, 0402, 5%, 1/16W	various
R2	33kΩ	Resistor, Chip, 0402, 5%, 1/16W	various
LI	18nH	Inductor, 0603, 5%, Ceramic	various
C4	1uF	Cap, Chip, 0402, 10%, 10V, X5R	
C1 C2 C3	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various

High Linearity, Low Noise Gain Block Chip, 0.02 - 6 GHz

Pin Definition		
Bonding point number	Function Symbol	Functional Description
2	RF IN	RF input port, impedance 50ohm , requires external DC blocking capacitor
6	Shut Down	Shutdown control port
7	RF OUT / DC Bias	RF output port, impedance 50ohm, amplifier leakage bias, bias the circuit at the output end through external current-choking inductor and bias resistor, external DC blocking capacitor is required
1, 3, 4, 5, 8	NC	No welding required
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Use restriction parameter ¹	
Collector voltage: +6V	Input power: +23dBm
Operating temperature: -40 ~ +70 ° C	Storage Temperature: -65 ~ +150°C

【2】 Exceeding any of these maximum limits may cause permanent damage.

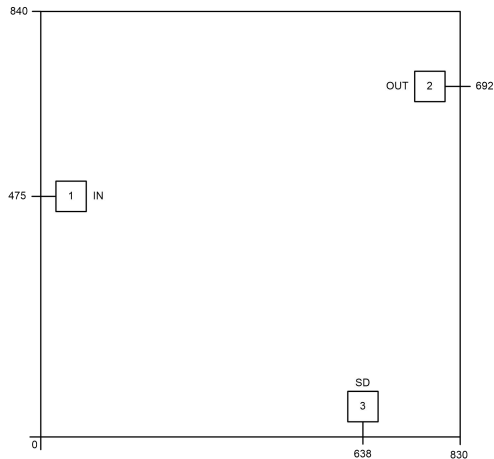
Environmental conditions		
Parameter	Grade	Standard
ESD – Human Body Model (HBM)	1A	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	C3	ESDA / JEDEC JS-001-2014
MSL – Moisture Sensitivity Level	LEVEL 1	IPC/JEDEC J-STD-020

Precautions for use

- Plastic package material : Low-pressure injection molding plastic that meets ROHS specifications
- Lead frame material: copper alloy
- Lead surface plating: 100% matte tin
- Maximum reflow peak temperature: 260 °C

High Linearity Low Noise Gain Amplifier , 200 - 6000MHz

DIE appearance structure



DIE pad definition

Bonding point number	Function Symbol	Functional Description
1	RF IN	RF input port, impedance 50ohm , requires external DC blocking capacitor
3	Shut Down	Shutdown control port
2	RF OUT / DC Bias	RF output port, impedance 50ohm, amplifier leakage bias, bias the circuit at the output end through external current-choking inductor and bias resistor, external DC blocking capacitor is required
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

DIE recommended assembly drawing

