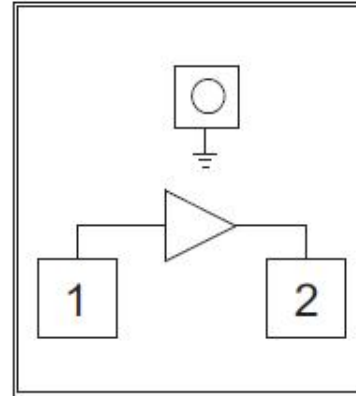


High Linearity, Low Noise Gain Block Chip, 0.05-4GHz

Performance characteristics

- Frequency range: 0.05 - 4 GHz
- Small signal gain: 14dB
- Gain flatness: ± 0.15 dB (0.5 ~3.5GHz)
- Noise figure: 2.5dB
- P-1 dB: 19dBm
- OIP3: 35.5dBm@ Pout=+4dBm/tone, $\Delta f=1$ MHz
- Current : 85mA
- ESD: 500V
- 50Ohm input / output
- Chip size: 1.18 x 0.83 x 0.1 mm

Functional Block Diagram



Product Introduction

The GHLN-9028B-D is a GaAs monolithic amplifier operating from 0.05-4GHz. The circuit is biased via an external choke inductor at the output and provides 14dB gain, +19dBm P-1dB output power and + 35dBm output O IP3 at 85mA operating current .

Use restriction parameter ¹

Collector voltage	+7V
Input power	+23dBm
Operating Current	110mA
Operating temperature	-40 ~ +10 5 °C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

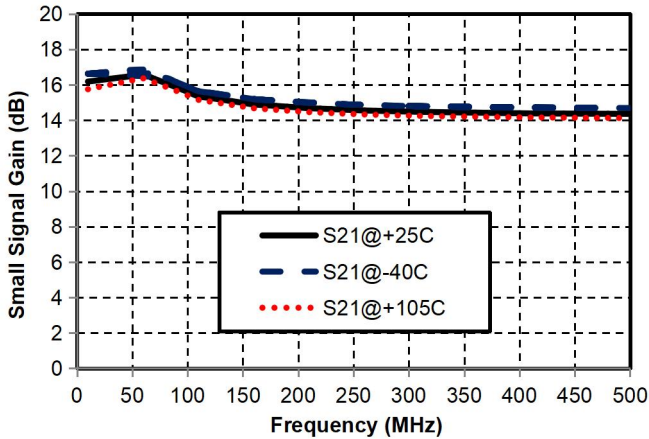
Electrical performance parameters (TA = +25°C , Vcc = +5V)

Index	Minimum	Typical Value	Maximum	Unit
Frequency Range	0.05-4			GHz
Small Signal Gain		14		dB
Gain flatness (0.5~3.5GHz)		± 0.15		dB
Input return loss		15	-	dB
Output return loss		12	-	dB
Reverse Isolation	-	21	-	dB
P-1 dB	-	19	-	dBm
OIP3 @@ Pout=+4dBm/tone, $\Delta f=1$ MHz		35		dBm
Noise Figure	-	2.5		dB
Quiescent Current	-	85	-	mA

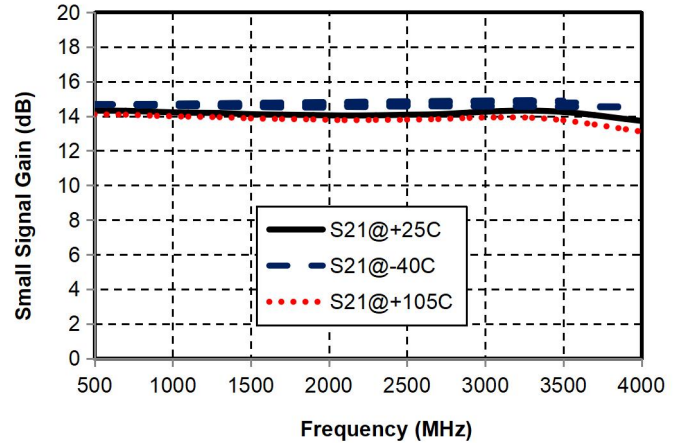
High Linearity, Low Noise Gain Block Chip, 0.05-4GHz

Main index test curve

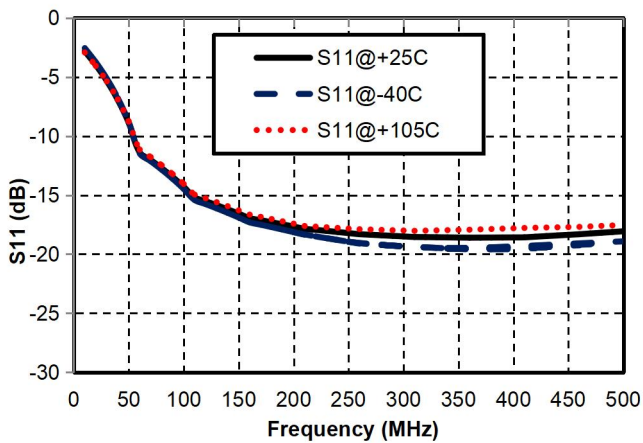
Gain vs. Frequency @50~500MHz



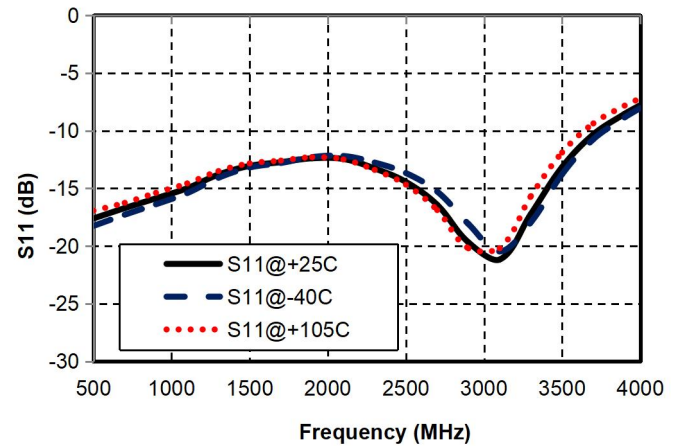
Gain vs. Frequency @500~4000MHz



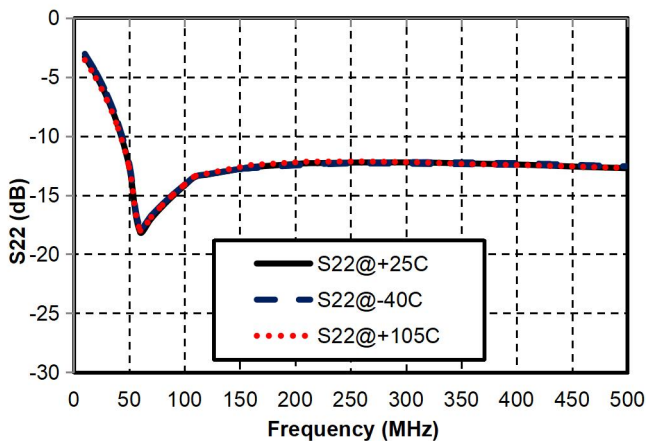
Input Return Loss vs. Frequency @50~500MHz



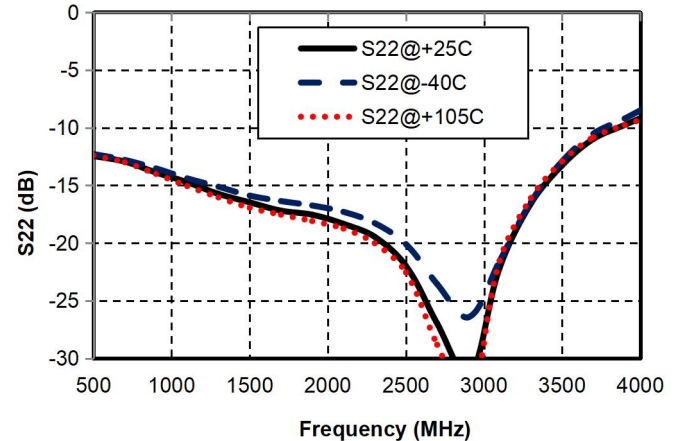
Input Return Loss vs. Frequency @500~4000MHz



Output return loss vs. frequency @50~500MHz

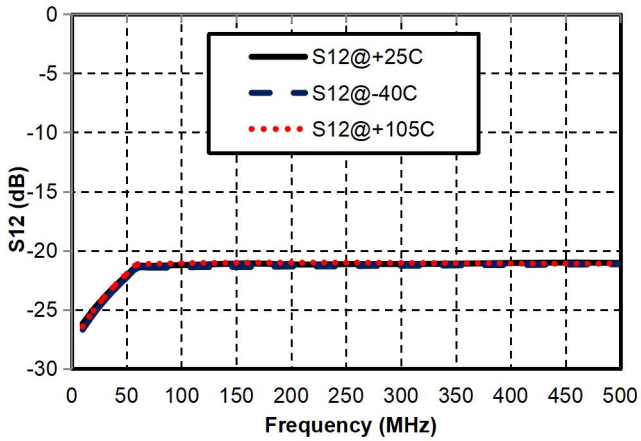


Output return loss vs. frequency @500~4000MHz

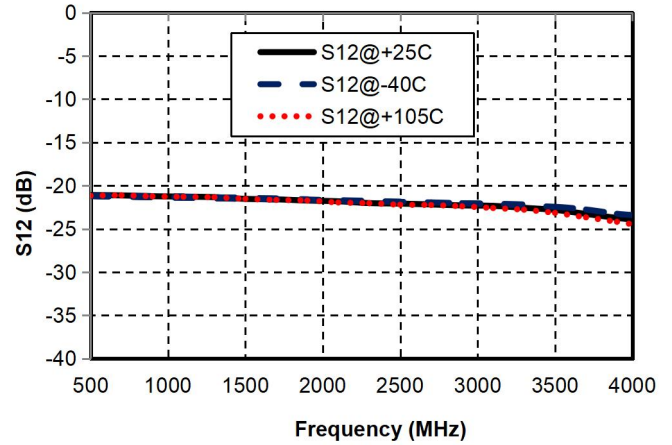


High Linearity, Low Noise Gain Block Chip, 0.05-4GHz

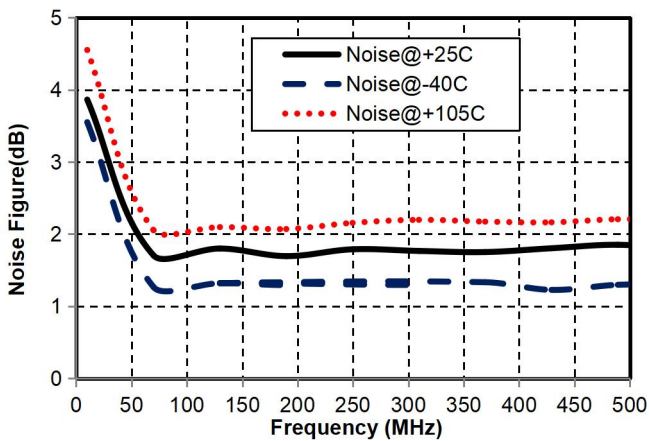
Reverse Isolation vs. Frequency @ 50~500MHz



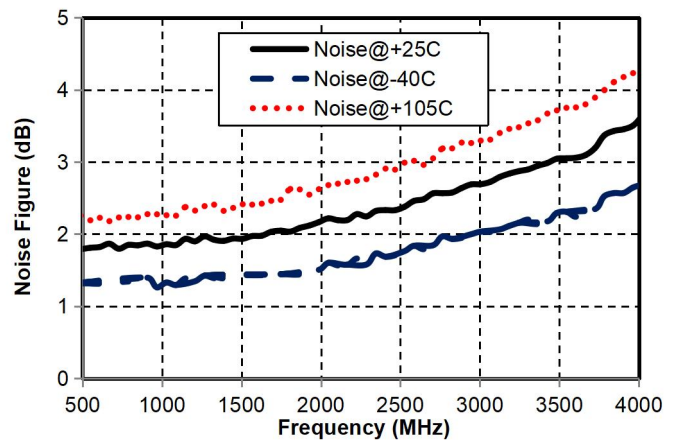
Reverse Isolation vs. Frequency @ 500~4000MHz



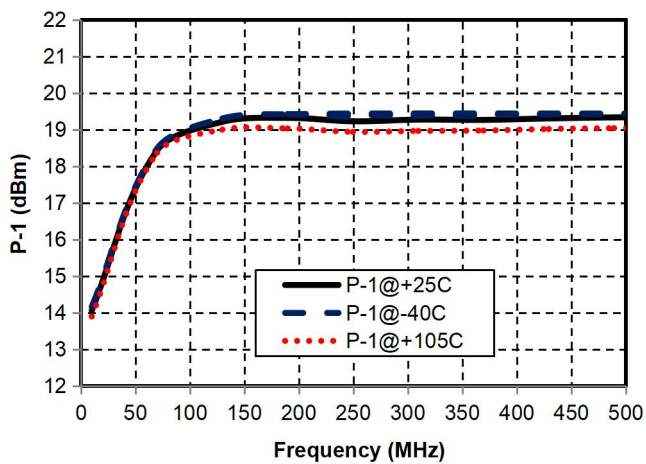
Noise Figure vs. Frequency @50~500MHz



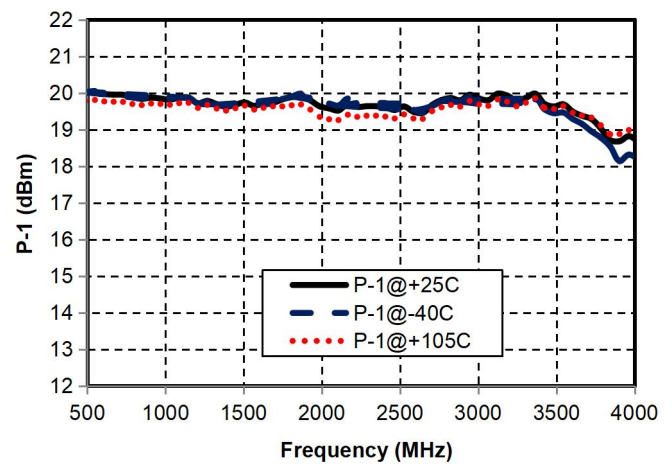
Noise Figure vs. Frequency@500~4000MHz



P-1 vs. Frequency @50~500MHz

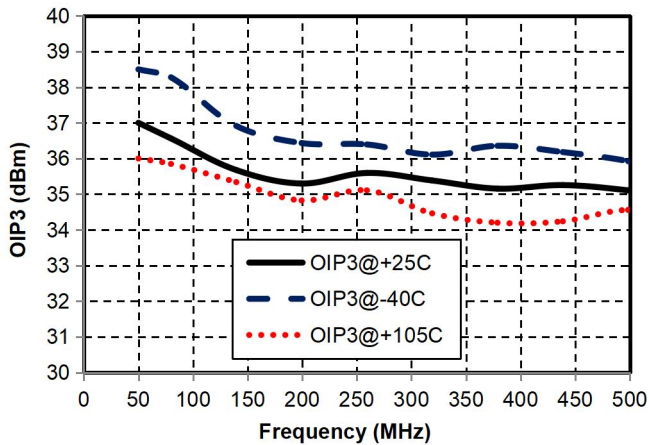


P-1 vs. Frequency @ 500~4000MHz

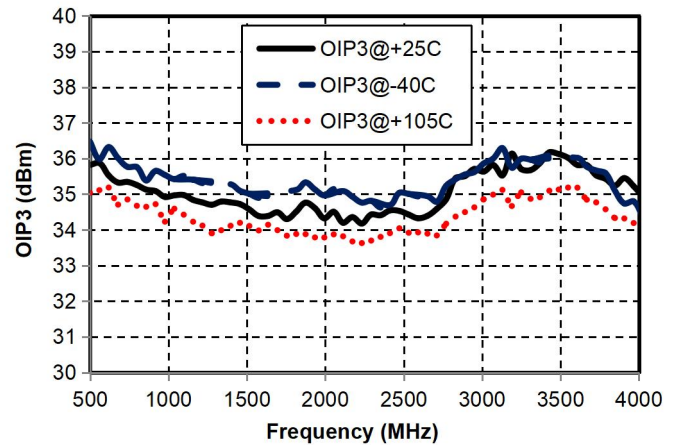


High Linearity, Low Noise Gain Block Chip, 0.05-4GHz

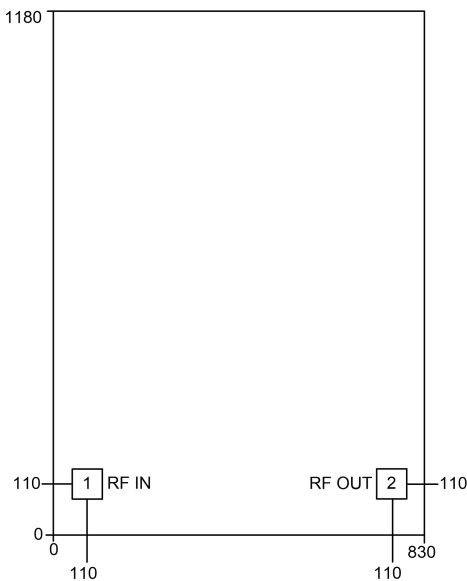
OIP3 vs. Frequency @ 50~500MHz



OIP3 vs. Frequency @ 500~4000MHz



Appearance structure

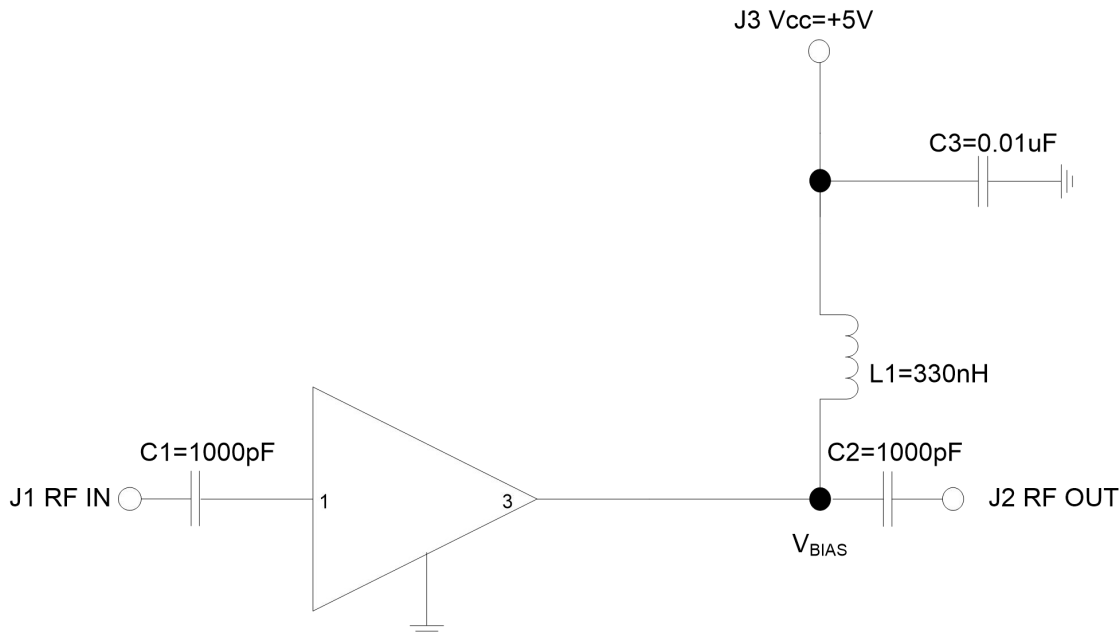


All units in the figure are micrometers

Bonding point number	Function Symbol	Functional Description
1	RFIN	RF input, external DC blocking capacitor is required
2	RFOUT	RF output and chip DC bias, bias the circuit at the output end through external choke inductor and bias resistor, and require external DC blocking capacitor
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

High Linearity, Low Noise Gain Block Chip, 0.05-4GHz

Recommended circuit diagram (50~500MHz)



Recommended circuit diagram (500~4000MHz)

