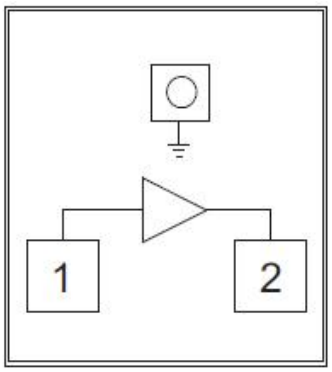
GHLN-015A

High Linearity, Low Noise Gain Block Chip, DC-2GHz

Performance characteristics

- Working frequency: DC - 2GHz
- Noise figure: 1.0 dB
- Small signal gain: 20dB
- Gain flatness: ± 0.5dB
- P-1dB: 19dBm
- OIP3: 24 dBm
- 50Ohm input and output
- +5V /15mA (static)
- DIE: 0.74 x 0.78 x0.1mm

Functional Block Diagram



Use restriction parameter [1]	
Input power	+23dBm
Operating Current	110mA
Operating temperature	-55 ~ + 105 °C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C , Vcc = +5V)				
Index	Minimum	Typical Value	Maximum	Unit
Frequency Range		DC-2		GHz
Small Signal Gain		20		dB
Gain Flatness		± 0.5		dB
Input return loss		14	-	dB
Output return loss		14	-	dB
Reverse Isolation	-	twenty four	-	dB
P-1 dB	-	19	-	dBm
OIP3 @with Pout=0dBm		twenty four		dBm
Noise Figure	-	1.0		dB
Quiescent Current	-	15	-	mA
Dynamic Current		45		mA

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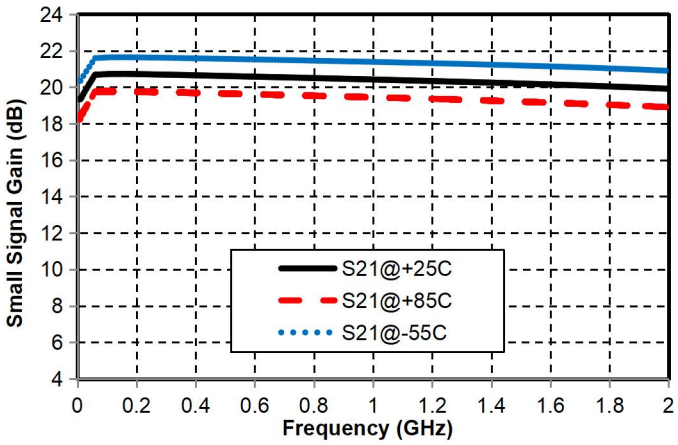
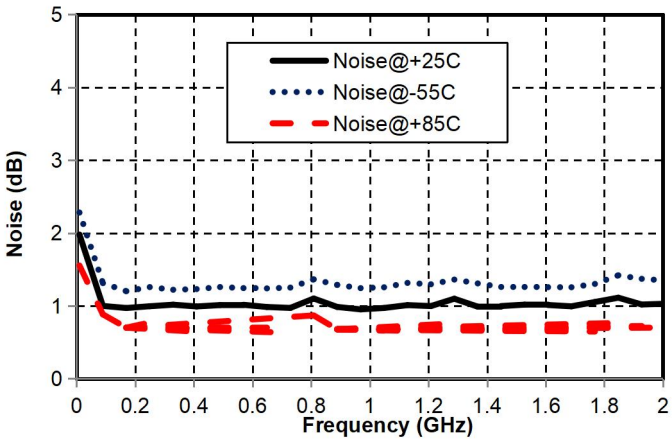
Main index test curve

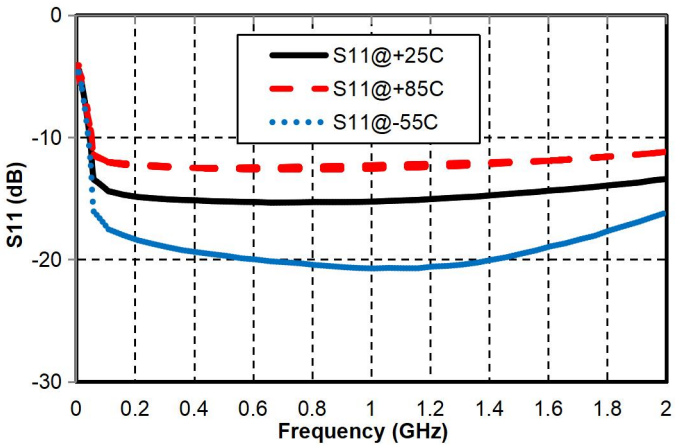
Gain vs. Frequency



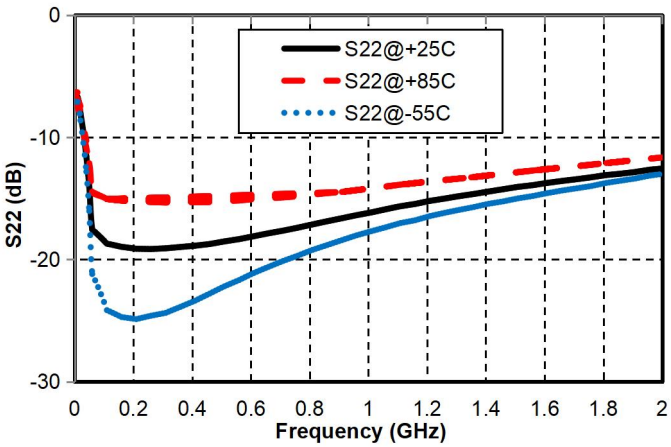
Noise Figure vs. Frequency



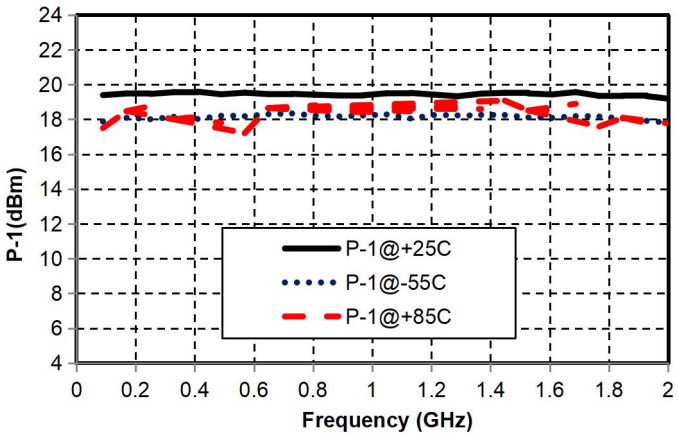
Input Return Loss vs. Frequency



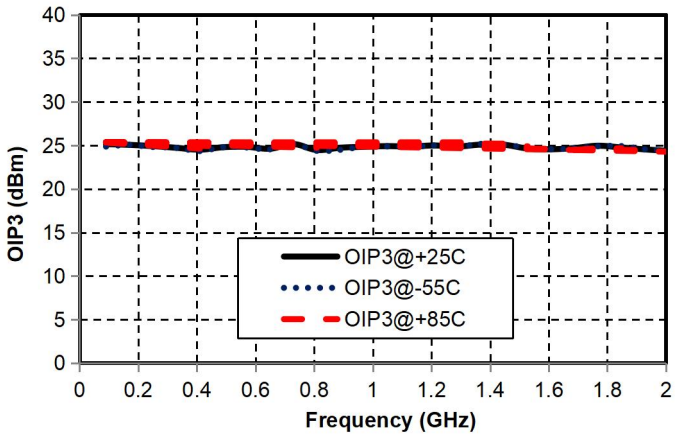
Output Return Loss vs. Frequency



P-1dB vs. Frequency



OIP3 vs. Frequency (Pout=0dBm)



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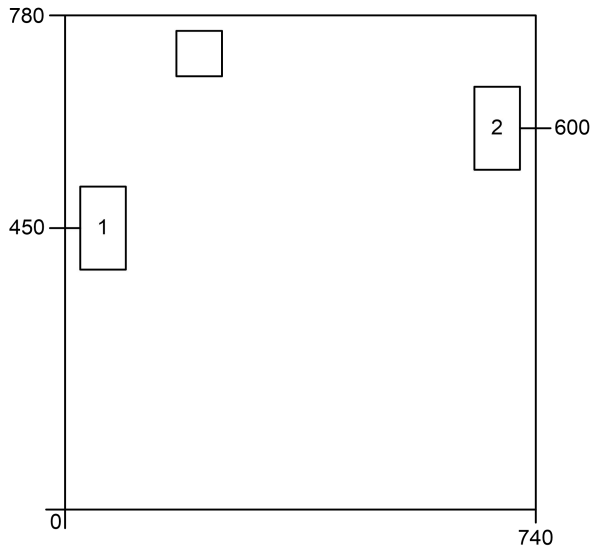
Appearance structure



Bonding point number	Function Symbol	Functional Description
1	RFIN	RF input, external DC blocking capacitor is required
2	RFOUT	RF output and chip DC bias, bias the circuit at the output end through external choke inductor and bias resistor, and require external DC blocking capacitor
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Recommended circuit diagram