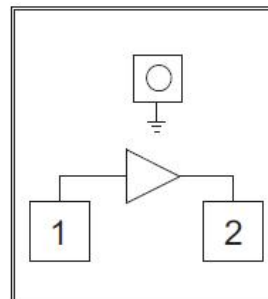


High Linearity, Low Noise Gain Block Chip, 0.1- 3.5GHz

Performance characteristics

- Operating frequency: 0.1 - 3.5 GHz
- Noise figure: 1.0 dB
- Small signal gain: 22dB
- P-1dB: 17.5dBm
- OIP3: 35 dBm
- 50Ohm input and output
- + 3V / 50mA
- DIE: 0.8 x 0.75 x0.1mm

Functional Block Diagram



Use restriction parameter ¹

Input power	+20dBm
Operating Current	100mA
Operating temperature	-55 ~ + 105 °C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

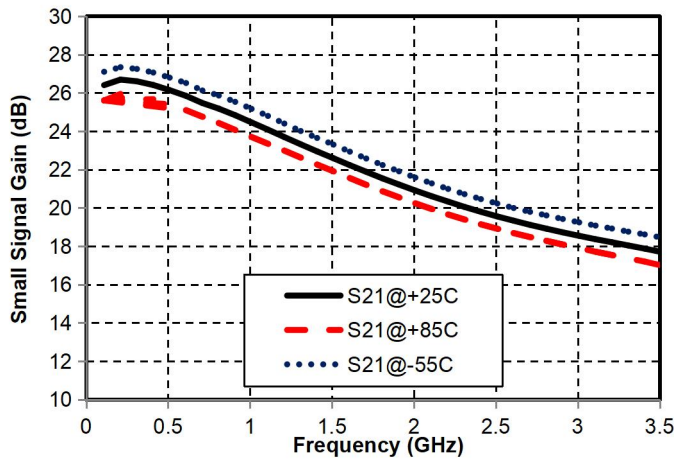
Electrical performance parameters (TA = +25°C , V_{CC} = +3V, R = 0Ω)

Index	Minimum	Typical Value	Maximum	Unit
Frequency Range	0.1-3.5			G Hz
Small Signal Gain	-	twenty two	-	dB
Input return loss	-	14	-	dB
Output return loss	-	10	-	dB
Reverse Isolation	-	29	-	dB
P-1 dB	-	17.5	-	dBm
Psat	-	19	-	dBm
OIP3 @with Pout=0dBm	-	35	-	dBm
Noise Figure	-	1.0	-	dB
Quiescent Current	-	50	-	mA

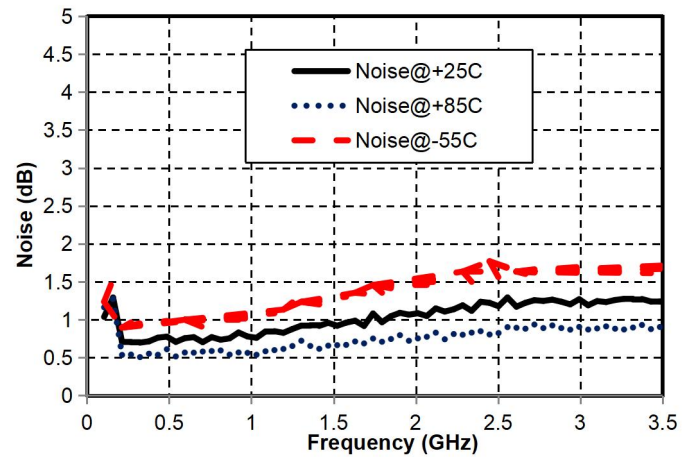
High Linearity, Low Noise Gain Block Chip, 0.1-3.5GHz

Main index test curve

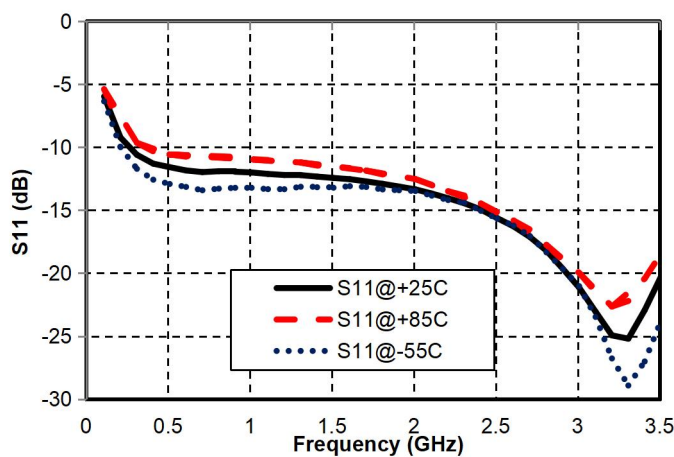
Gain vs. Frequency



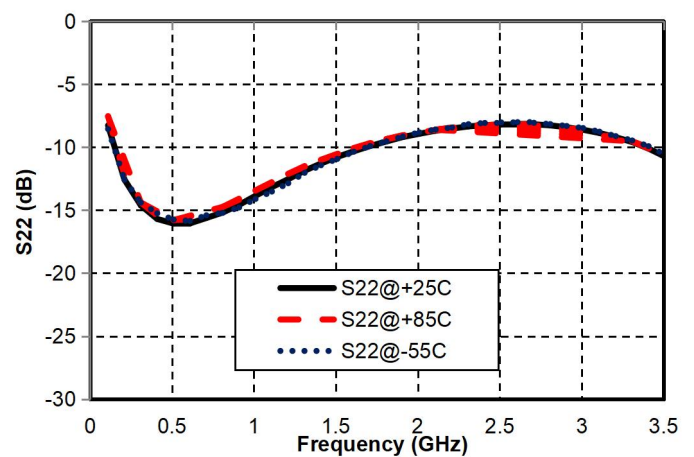
Noise Figure vs. Frequency



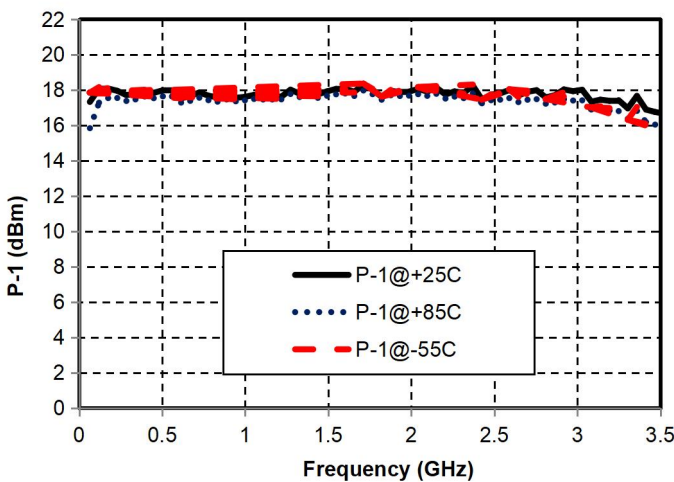
Input Return Loss vs. Frequency



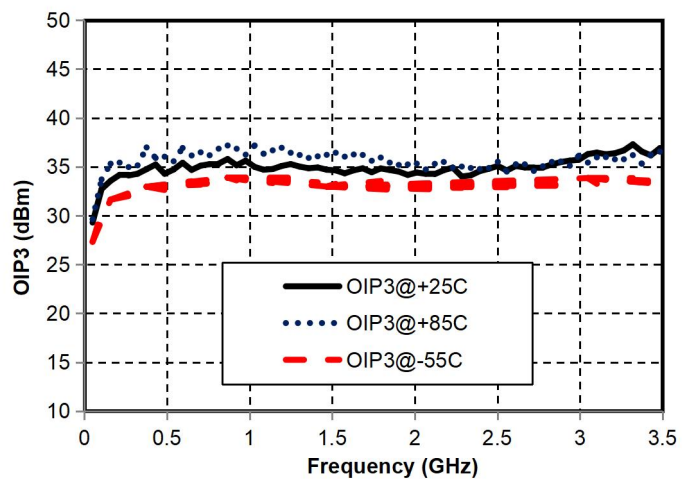
Output Return Loss vs. Frequency



P-1dB vs. Frequency

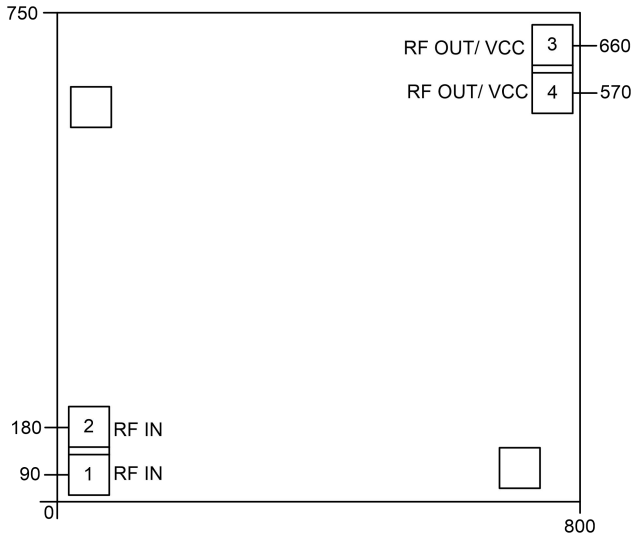


OIP3 vs. Frequency (Pout=0dBm)



High Linearity, Low Noise Gain Block Chip, 0.1-3.5GHz

Appearance structure



Bonding point number	Function Symbol	Functional Description
1, 2	RFIN	RF input, external DC blocking capacitor is required
3,4	RFOUT	RF output and chip DC bias, bias the circuit at the output end through external choke inductor and bias resistor, and require external DC blocking capacitor
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

*It is recommended to use gold wire to connect RFIN ports 1 and 2 , and gold wire to connect RFOUT/V CC ports 3 and 4 .

Recommended circuit diagram

