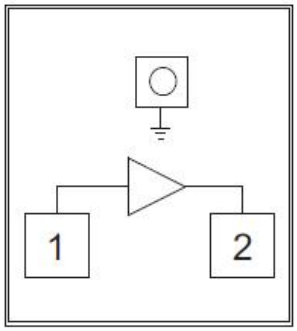
# GHLN-010A

## High Linearity, Low Noise Gain Block chip, 0.1-3GHz

### Performance characteristics

- Working frequency band : 0.1-3GHz
- Noise figure: <1.0dB @100MHz~2GHz
- Small signal gain: 25.5dB@1GHz
- P-1dB: 17dBm Typ
- OIP3: 33 dBm
- 50Ohm input and output
- + 3V / 60mA
- DIE: 0.83 x 0.93 x0.1mm

### Functional Block Diagram




| Use restriction parameter [1] | |
|---|---|
| Collector voltage | +6 V |
| Input power | +20dBm |
| Operating Current | 80mA |
| Operating temperature | -55 ~ + 105 °C |
| Storage temperature | -65 ~ +150°C |

【1】 Exceeding any of these maximum limits may cause permanent damage.

| Electrical performance parameters ( TA = +25°C, Vd = +3V, 50Ω system) | | | | | |
|---|---|---|---|---|---|
| Index | Test Conditions | Minimum | Typical Value | Maximum | Unit |
| Frequency Range | | 0.1 | | 3 | GHz |
| Test frequency | | | 1 | | GHz |
| Small Signal Gain | | | 25.5 | | dB |
| Input return loss | | | 12 | | dB |
| Output return loss | | | 14 | | dB |
| P-1 | | | 17.5 | | dBm |
| OIP3 | Pout = 0 dBm/tone, Δf = 1 MHz | | 34 | | dBm |
| Noise Figure | Without de-embedding, the estimated evaluation board loss is 0.15dB@1.0G | | 0.65 | | dB |
| Current | Static | | 60 | | mA |

*The noise figure result does not deduct the input loss of the test DEMO board .

Add: 101 cecil street #14-10, tong eng building singapore 069533
Email: info@standardcircuit.com
Web: www.standardcircuit.com
Tel: +65 82613258

# GHLN-010A

## High Linearity, Low Noise Gain Block chip, 0.1-3GHz

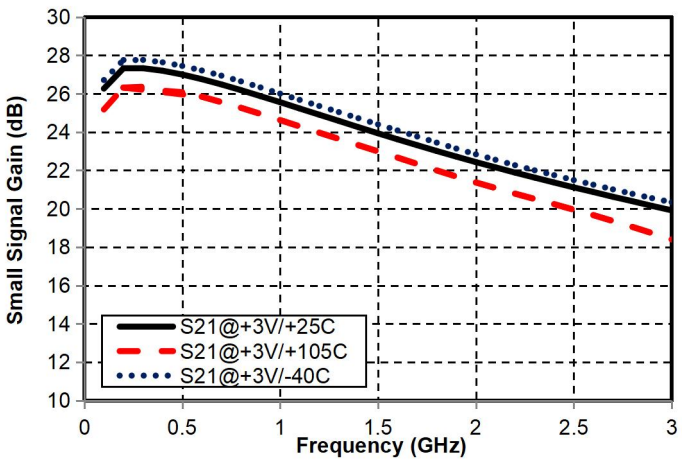
### 0.1-3GHz electrical performance parameters

| Electrical performance parameters ( TA = +25°C, Vd = +3V, 50Ω system, 60mA ) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Index | Typical Value | | | | | | Unit |
| Test frequency | 0.1 | 0.4 | 0.9 | 1.9 | 2.45 | 3.5 | MHz |
| Small Signal Gain | 2 6.0 | 27.0 | 25.5 | 22.5 | 21.0 | 1 8.5 | dB |
| Input return loss | 6.0 | 12.0 | 12.0 | 12.0 | 12.0 | 21.0 | dB |
| Output return loss | 7.0 | 15.0 | 15.0 | 9.0 | 8.0 | 9.5 | dB |
| P-1 | 18.0 | 17.5 | 17.5 | 17.5 | 17.5 | 16.0 | dBm |
| OIP3* | 32.0 | 36.0 | 34.0 | 34.5 | 33.0 | 30.5 | dBm |
| Noise Figure** | 1.0 | 0.6 | 0.7 | 1.0 | 1.2 | 2.2 | dB |

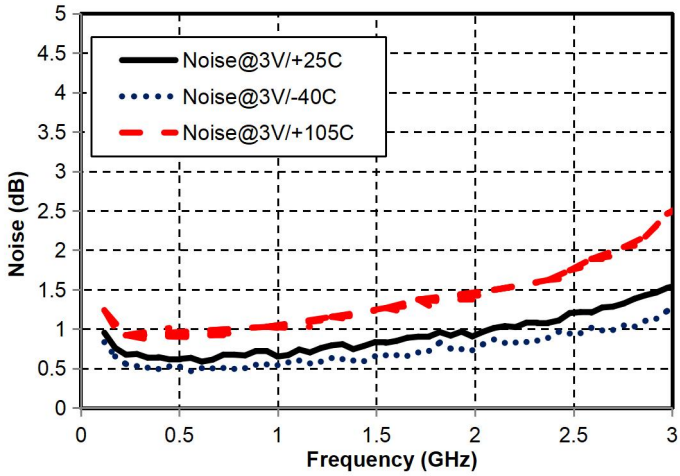
* Pout=+ 0dBm /tone, Δf =1MHz .

** Noise figure results do not deduct the input loss of the test DEMO board .

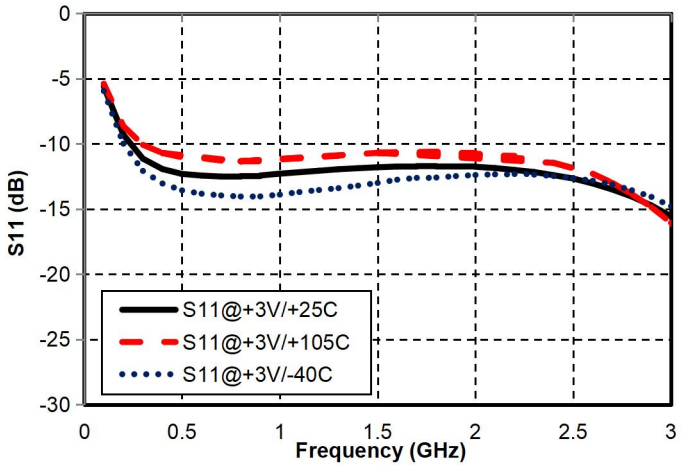
Small Signal Gain vs. Frequency



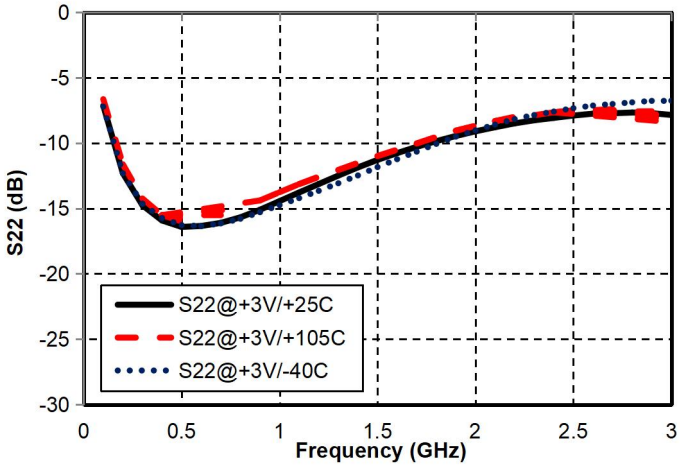

Noise Figure vs. Frequency




Input Return Loss vs. Frequency




Output Return Loss vs. Frequency

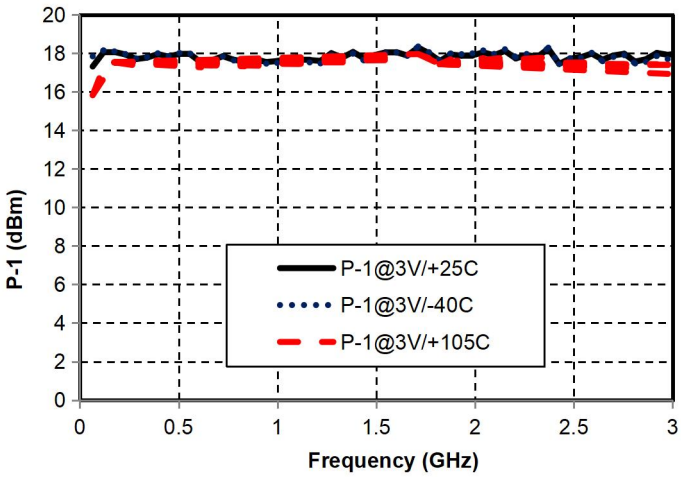




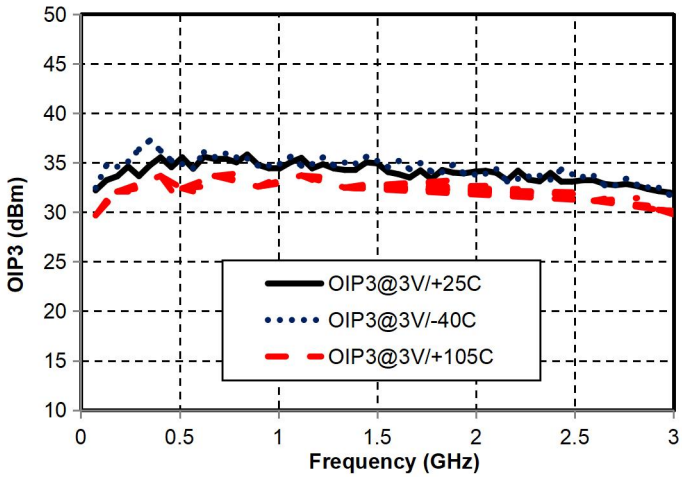
Add: 101 cecil street #14-10, tong eng building singapore 069533
Email: info@standardcircuit.com
Web: www.standardcircuit.com
Tel: +65 82613258

## High Linearity Low Noise Gain Amplifier, 0.1-3GHz

P-1dB vs. Frequency



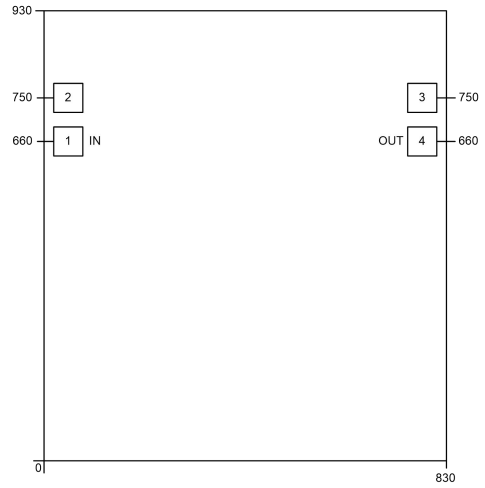

OIP3 vs. Frequency



# GHLN-010A

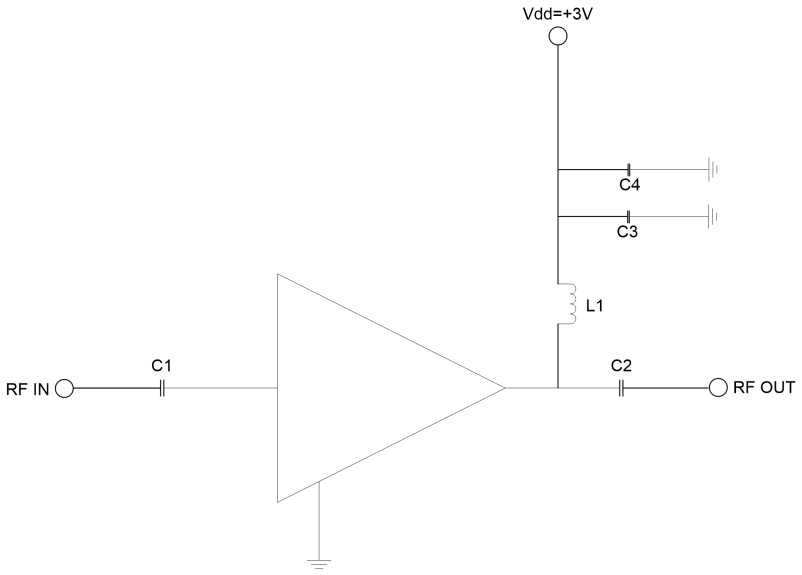
## High Linearity Low Noise Gain Amplifier, 0.1-3GHz

### Appearance structure




| Bonding point number | Function Symbol | Functional Description |
|---|---|---|
| 1 | RFIN | RF input, external DC blocking capacitor is required |
| 4 | RFOUT | RF output and chip DC bias, bias the circuit at the output end through external choke inductor and bias resistor, and require external DC blocking capacitor |
| Chip bottom | GND | The bottom of the chip needs to be well grounded to RF and DC |

### Recommended circuit diagram




C1 , C2, C3 = 1000pF ; C4 = 1uF; L1 = 82nH ; capacitance and inductance can be adjusted according to different application frequency bands.


Add: 101 cecil street #14-10, tong eng building singapore 069533
Email: info@standardcircuit.com
Web: www.standardcircuit.com
Tel: +65 82613258