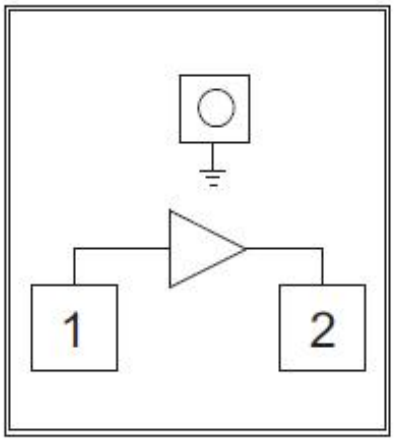
GHLN- 009A

High Linearity, Low Noise Gain Block Chip, 0.05-6GHz

Performance characteristics

- Frequency range: 0.05-6 GHz
- Small signal gain: >20dB (full frequency band)
- Gain flatness: ± 0.7 dB (0.05~1.5G, 1.5~3.6G, 3.5~6.0GHz)
- Noise figure: 0.8dB@1.2GHz ; 1.3dB@5.0GHz
- P-1dB: 19.5dBm@1.2GHz ; 18.5dBm@5.0GHz
- OIP3: 35dBm@1.2GHz ; 30.5dBm@5.0GHz
- Power supply: +5V/85mA (quiescent current)
- Support +3V ~ +5V operation
- ESD: 500V
- 50Ohm input/output
- Chip size: 0.79 x 0.93 x 0.1 mm

Functional Block Diagram



Use restriction parameter [1]

Collector voltage	+10 V
Input power	+20dBm
Operating Current	120mA
Operating temperature	-55 ~ + 105 °C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of these maximum limits may cause permanent damage.

Electrical performance parameters (TA = +25°C, Vd = +5V, 50Ω system)

Index	Test Conditions	Minimum	Typical Value	Maximum	Unit
Frequency Range		50		6000	MHz
Small Signal Gain			21		dB
*Noise Figure			1.0		dB
Input return loss			12		dB
Output return loss			14		dB
P-1 (0.05 ~ 1.5 GHz)			20		dBm
P-1 (1.5 ~ 3.8 GHz)			20		dBm
P-1(3.8~6.0GHz)			17		dBm
OIP3 (0.05 ~ 1.5 GHz)	Pout=+ 5 dBm /tone, Δf = 5 MHz		36		dBm
OIP3 (1.5 ~ 3.8GHz)			33		dBm
OIP3(3.8 ~6.0GH z)			28		dBm
OIP2 (LOWER)	Pout=+ 5 dBm /tone, Δf = 53 MHz		39		dBm
OIP2 (UPPER)			38		dBm
Quiescent Current			85		mA

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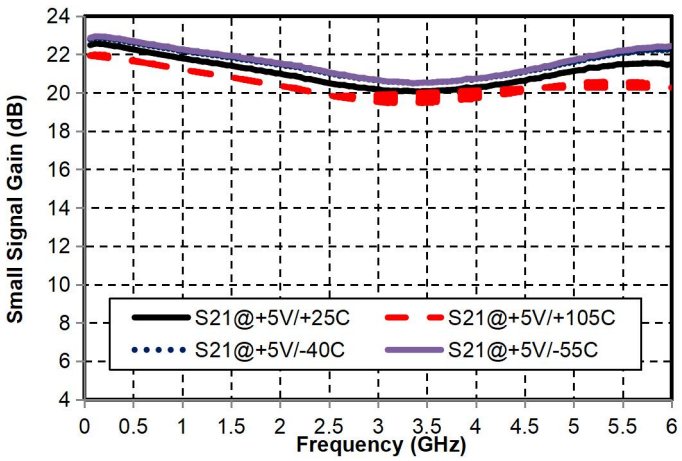
50M-6000M electrical performance parameters

Electrical performance parameters (TA = +25°C, VDD = +5V, 50Ω system, 90mA)												
Index	Typical Value											unit
Test frequency	100	500	900	1200	1900	2300	3000	3600	4000	5000	6000	MHz
Small Signal Gain	22.5	22.0	21.5	21.5	21.0	20.5	20.0	20.0	20.0	21.0	21.5	dB
Input return loss	15.0	16.0	15.5	14.5	12.5	10.5	10.0	11.5	13.0	13.5	7.0	dB
Output return loss	21.0	22.0	18.0	16.0	12.5	10.0	8.0	8.0	9.0	16.0	14.0	dB
P-1	19.5	20.0	20.0	20.0	20.0	20.0	19.5	19.5	18.5	17.0	16.0	dBm
OIP3	37.0	37.0	36.5	35.0	34.5	34.0	32.0	31.0	30.0	28.0	27.0	dBm
Noise Figure*	0.8	0.6	0.65	0.7	0.8	0.8	0.9	1.0	1.0	1.3	1.7	dB

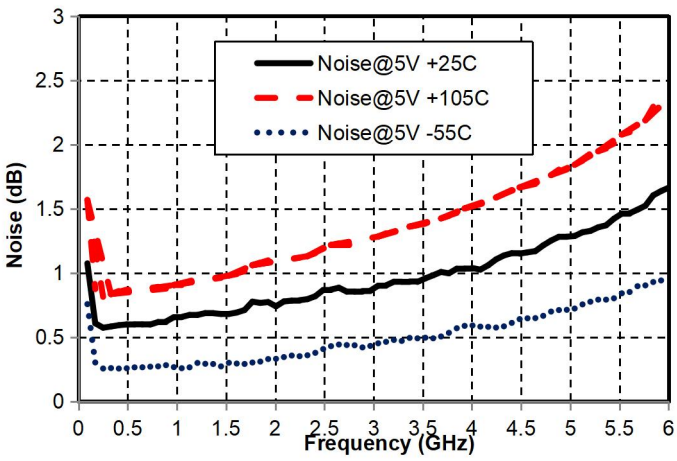
*The noise figure result does not deduct the input loss of the test DEMO board .

Main index test curve (TA = +25° C, VDD=+5V, 50Ω system)

Small Signal Gain vs. Frequency



Noise Figure vs. Frequency



Input Return Loss vs. Frequency

Output Return Loss vs. Frequency

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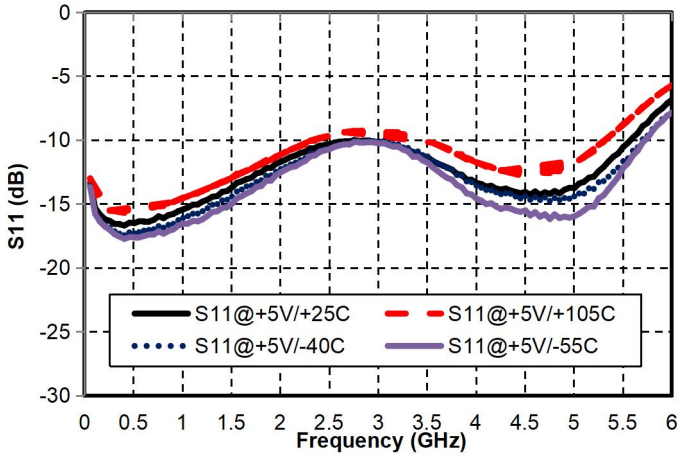

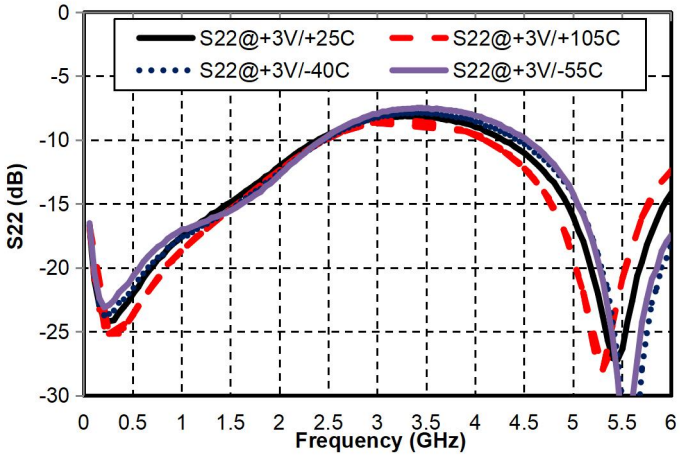

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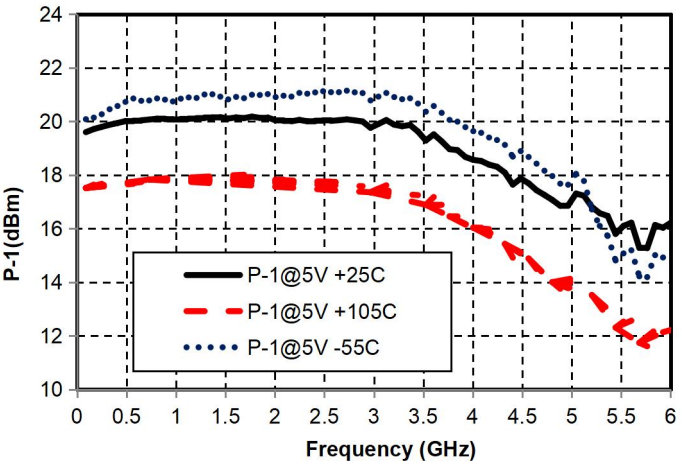
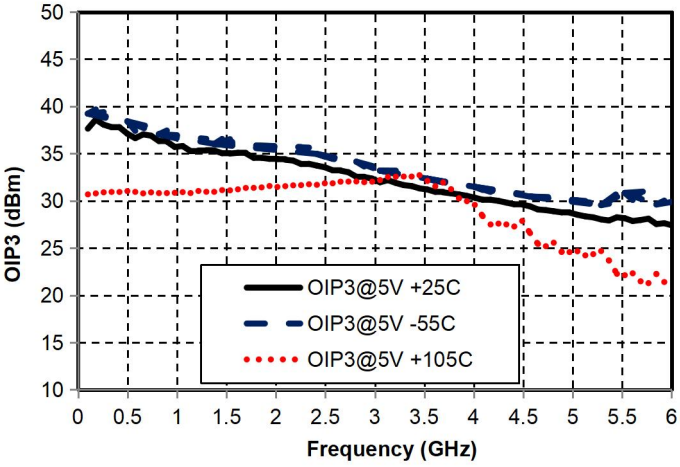
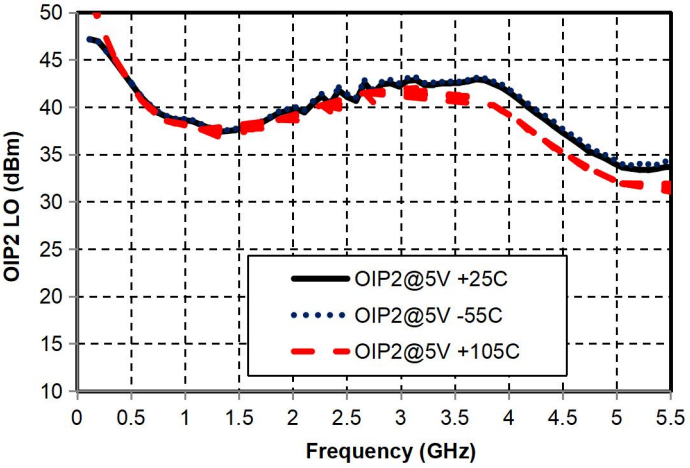
P-1dB vs. Frequency



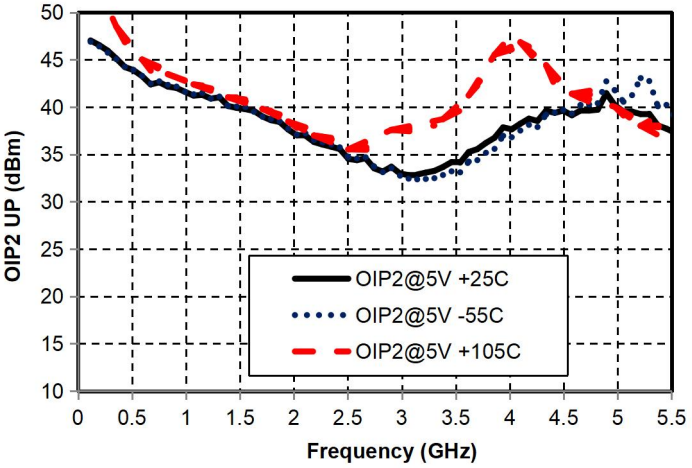
OIP3 vs. Frequency



OIP2 vs. Frequency (LOWER)



OIP2 vs. Frequency (UPPER)



Standard Circuit

GHLN- 009A

High Linearity, Low Noise Gain Block Chip, 0.05-6GHz

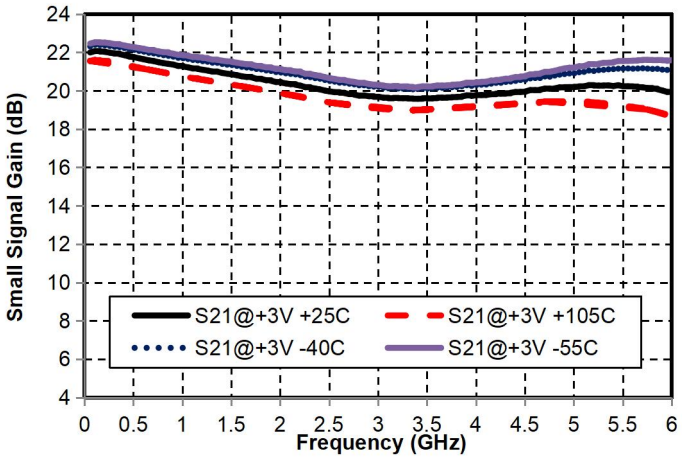
50M-6000M electrical performance parameters:

Electrical performance parameters (TA = +25° C, VDD = +3V, 50Ω system , 55mA)												
Index	Typical Value											unit
Test frequency	100	500	900	1200	1900	2300	3000	3600	4000	5000	6000	MHz
Small Signal Gain	22.0	21.5	21.0	21.0	20.5	20.0	19.5	19.5	19.5	20.0	20.0	dB
Input return loss	13.0	14.0	14.0	13.0	11.0	9.0	8.5	10.0	11.5	10.0	5.0	dB
Output return loss	20.0	20.0	19.0	17.0	13.5	11.0	9.0	9.0	9.5	15.0	14.0	dB
P-1	14.0	15.5	16.0	16.0	16.0	16.0	15.0	14.5	13.5	12.0	11.0	dBm
OIP3	28.0	29.5	29.5	29.5	30.0	30.5	30.5	30.0	26.5	20.0	19.0	dBm
Noise Figure*	0.6	0.6	0.6	0.6	0.7	0.7	0.8	0.9	1.0	1.2	1.6	dB

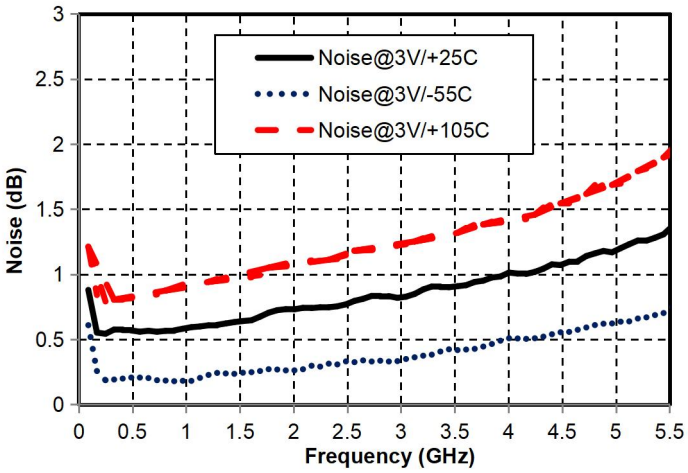
*The noise figure result does not deduct the input loss of the test DEMO board .

Main index test curve (TA = +25° C, VDD=+3V, 50Ω system)

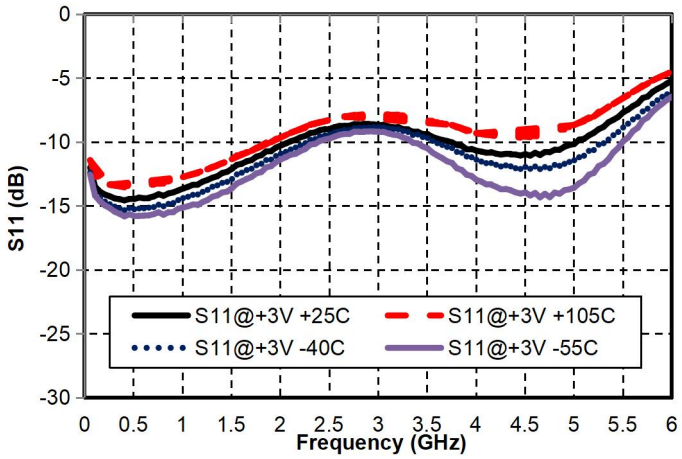
Small Signal Gain vs. Frequency



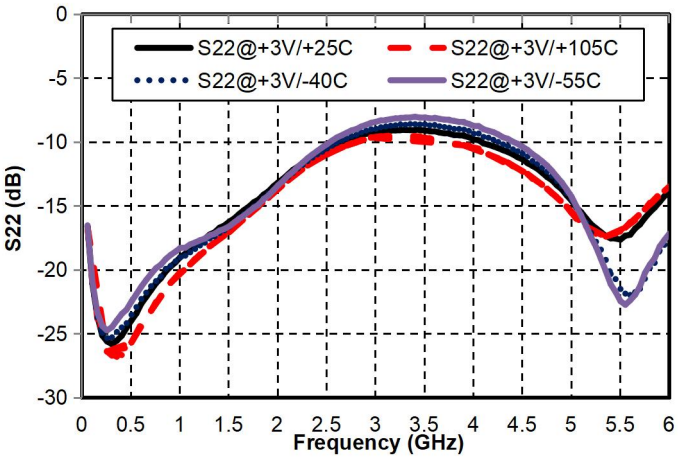
Noise Figure vs. Frequency



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



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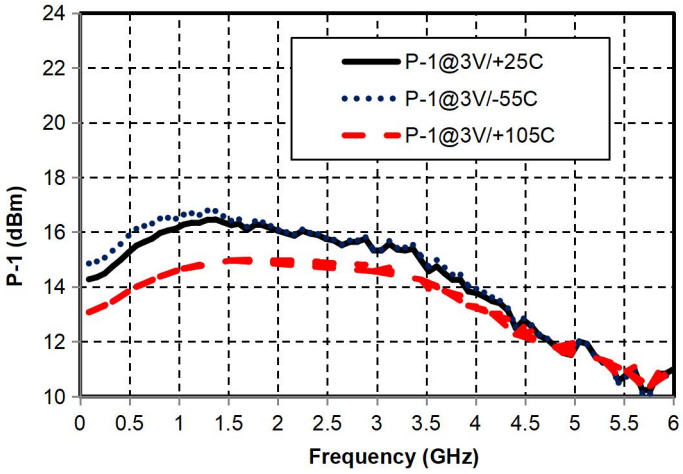
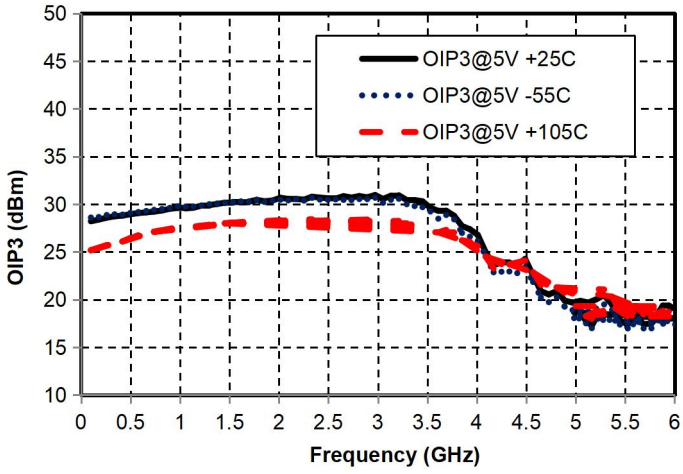
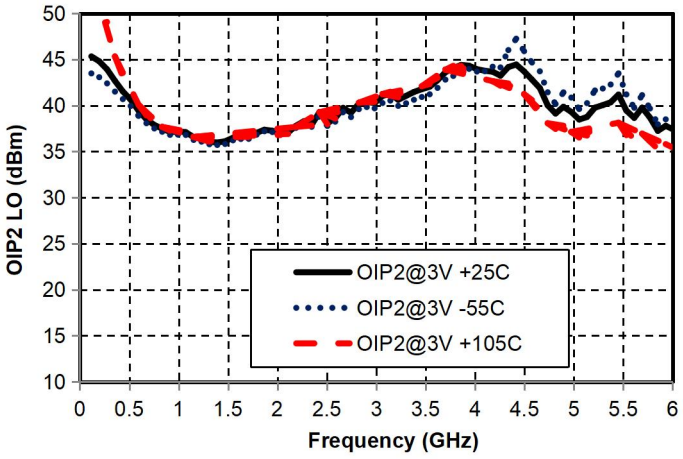
P-1dB vs. Frequency



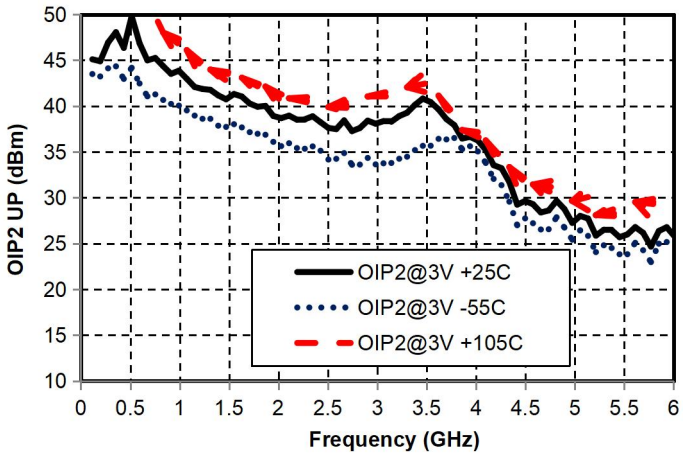
OIP3 vs. Frequency



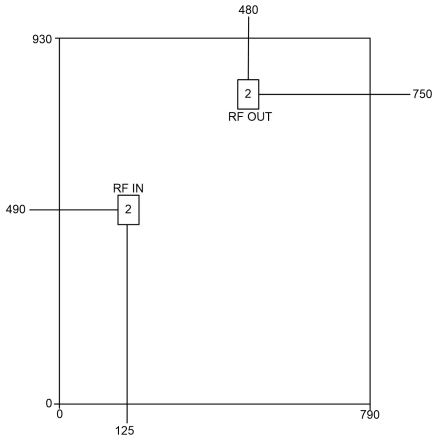
OIP2 vs. Frequency (LOWER)



OIP2 vs. Frequency (UPPER)



Appearance structure



All units in the figure are micrometers

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Bonding point number	Function Symbol	Functional Description
1	RFIN	RF input, external DC blocking capacitor is required
2	RFOUT	RF output and chip DC bias, bias the circuit at the output end through external choke inductor and bias resistor, and require external DC blocking capacitor
Chip bottom	GND	The bottom of the chip needs to be well grounded to RF and DC

Recommended circuit diagram