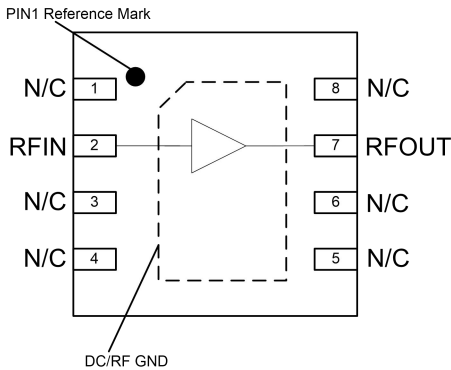


## High gain, high linearity, low noise gain amplifier , 50 - 6000 MHz

### Product Introduction

GHLN- 009A-DF2 is a low noise, high gain, high linearity MMIC RF amplifier. The amplifier has a full band bandwidth gain greater than 20 dB . This integrated circuit is widely used in cable TV, satellite and terrestrial TV applications, home gateways and cable TV modems. The amplifier is powered by a single + 5 V supply . GHLN-009A-DF2 is packaged in a standard DFN2X2 label, and all pins are equipped with ESD protection. The amplifier supports + 3V operation. The product quality level is industrial grade.

Block Diagram	Product Features
	<ul style="list-style-type: none"> <li>➤ Operating frequency: 50 - 6 000MHz</li> <li>➤ Small signal gain: &gt;20dB (full frequency band)</li> <li>➤ Gain flatness <math>\leq \pm 0.7</math> dB ( 0.05~1.5G, 1.5~3.6G , 3.5~ 6.0GHz )</li> <li>➤ Noise figure : 0.8dB@1.2GHz ; 1.3dB@5.0GHz</li> <li>➤ P-1dB : 19.5dBm@1.2GHz ; 18.5dBm@5.0GHz</li> <li>➤ OIP3: 35dBm@1.2GHz ; 30.5dBm@5.0GHz</li> <li>➤ 50Ohm input and output</li> <li>➤ +5V/85mA (Quiet Current)</li> <li>➤ Support +3V ~ +5V operation</li> <li>➤ 2x2 mm 8 Pin DFN plastic package</li> </ul>

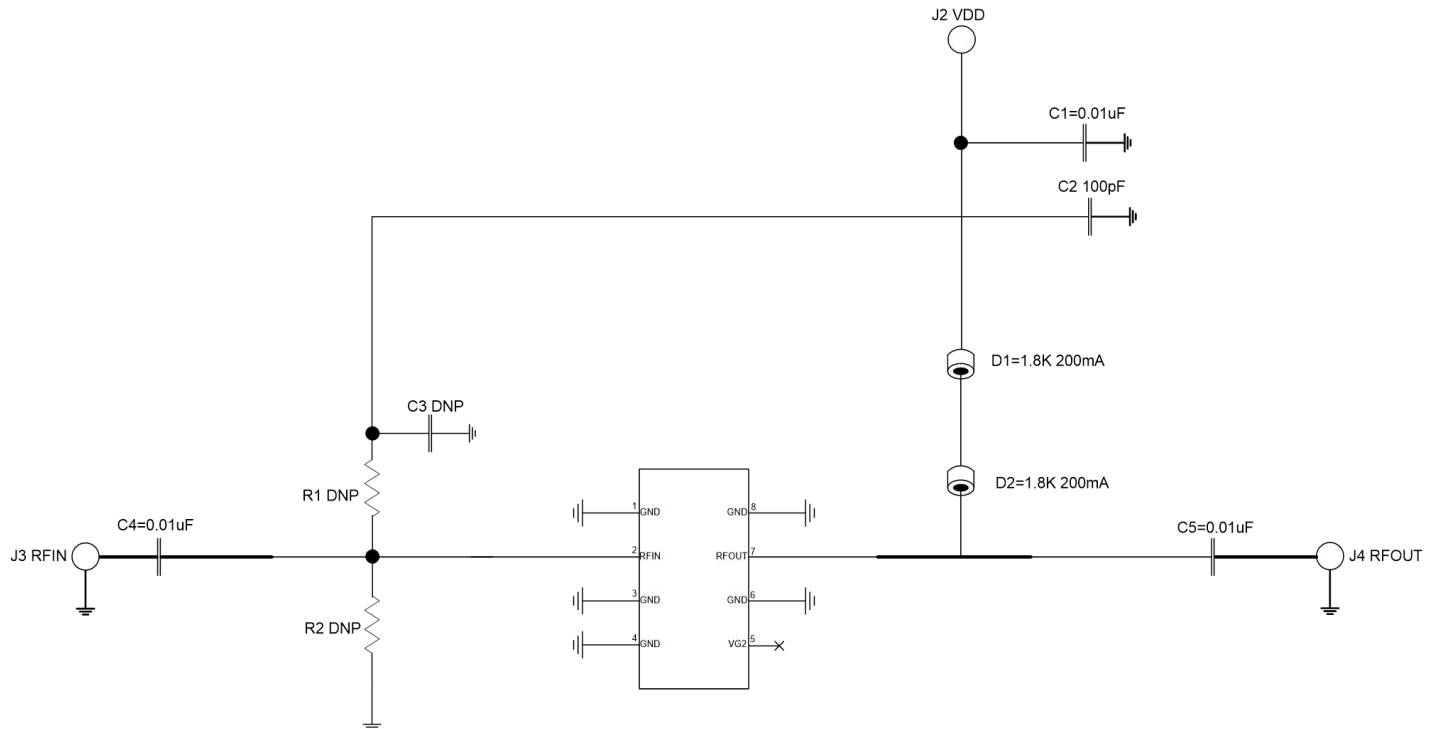
### Electrical performance parameters ( TA = +25°C, Vd=+5V, 50Ω system)

Index	Test Conditions	Minimum	Typical Value	Maximum	Unit
Frequency Range		50		6000	MHz
Small Signal Gain			21		dB
*Noise Figure			1.0		dB
Input return loss			12		dB
Output return loss			14		dB
P-1(0.05~1.5GHz)			20		dBm
P-1(1.5~3.8GHz)			20		dBm
P-1(3.8~6.0GHz)			17		dBm
OIP3(0.05~1.5GHz)	Pout=+5 dBm/tone, Δf=5MHz		36		dBm
OIP3 ( 1.5 ~ 3.8GHz )			33		dBm
OIP3( 3.8 ~6.0GHz )			28		dBm
OIP2 (LOWER)	Pout=+ 5 dBm/tone, Δf= 53 MHz		39		dBm
OIP2 (UPPER)			38		dBm
Quiescent Current			85		mA

\*The noise figure result does not deduct the input loss of the test DEMO board .

## High gain, high linearity, gain amplifier , 50 - 6000 MHz

50M-6000M recommended circuit diagram



### Notes

- 1、 D1, D2 provide DC bias path with RF isolation from the RF output path.
- 2、 C4, C5 provides DC blocking.
- 3、 R1, R2 and C3 are pullup/pulldown options that may be added from the input to VDD or to ground to increase linearity or shed power, trading off degraded noise figure and return loss. Device current can only be adjusted through R1 and R2.
- 4、 Pin5 is an internal gate voltage and may be left floating.

### Ingredients list

Designator	Description	Manufacturer	Part Number
D1 , D2	FER, BEAD, 1.8 KΩ, 5%, 200 mA, 0402	TDK	MMZ1005A182ET000
C1, C4, C5	CAP, 0.01 uF, 10 %,50 V, X8L, 0402	Murata Electronics	GCM155L81E103KA37D
J2	862000-055 Solder Turret, 0.062	Mouser Electronics	2533-0-00-44-00-00-07-
J3 , J4	RF SMA F, 50 Ω	Various	-
C2	100pF	Various	-
C3, R1, R2	Not Populated	-	-

## High gain, high linearity, gain amplifier , 50 - 6000 MHz

50M-6000M electrical performance parameters

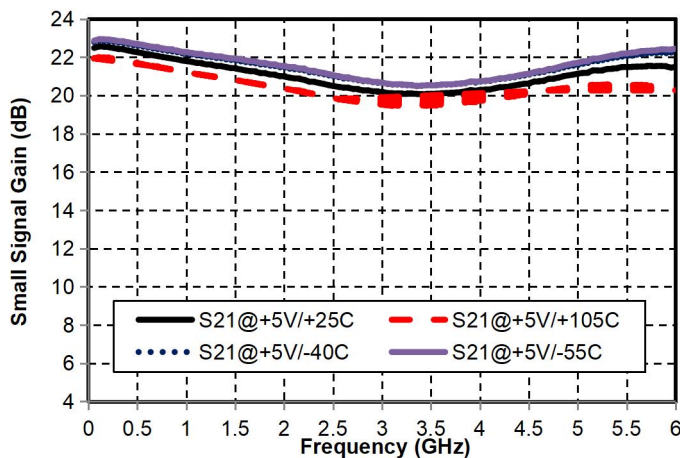
Electrical performance parameters ( TA = +25°C, VDD = +5V, 50Ω system, 90mA )

Index	Typical Value											Unit
Test frequency	100	500	900	1200	1900	2300	3000	3600	4000	5000	6000	MHz
Small Signal Gain	22.5	22.0	21.5	21.5	21.0	20.5	20.0	20.0	20.0	21.0	21.5	dB
Input return loss	15.0	16.0	15.5	14.5	12.5	10.5	10.0	11.5	13.0	13.5	7.0	dB
Output return loss	21.0	22.0	18.0	16.0	12.5	10.0	8.0	8.0	9.0	16.0	14.0	dB
P-1	19.5	20.0	20.0	20.0	20.0	20.0	19.5	19.5	18.5	17.0	16.0	dBm
OIP3	37.0	37.0	36.5	35.0	34.5	34.0	32.0	31.0	30.0	28.0	27.0	dBm
Noise Figure*	0.8	0.6	0.65	0.7	0.8	0.8	0.9	1.0	1.0	1.3	1.7	dB

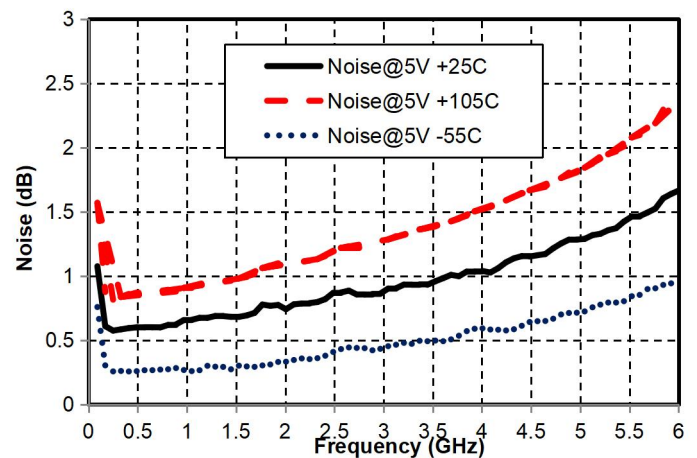
\*The noise figure result does not deduct the input loss of the test DEMO board .

Main index test curve ( TA = +25°C, VDD=+5V, 50Ω system)

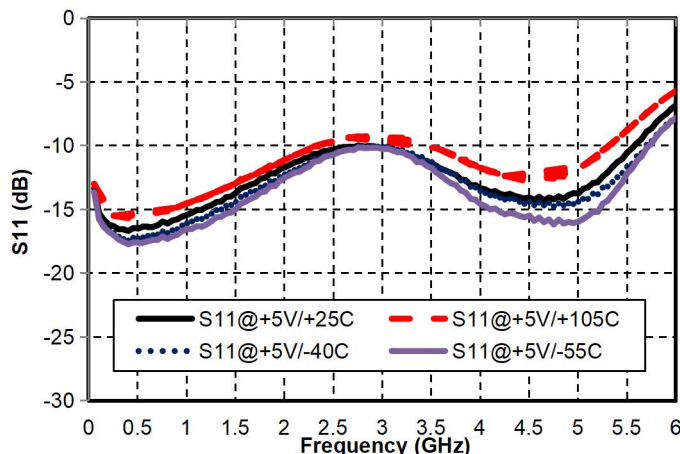
Small Signal Gain vs. Frequency



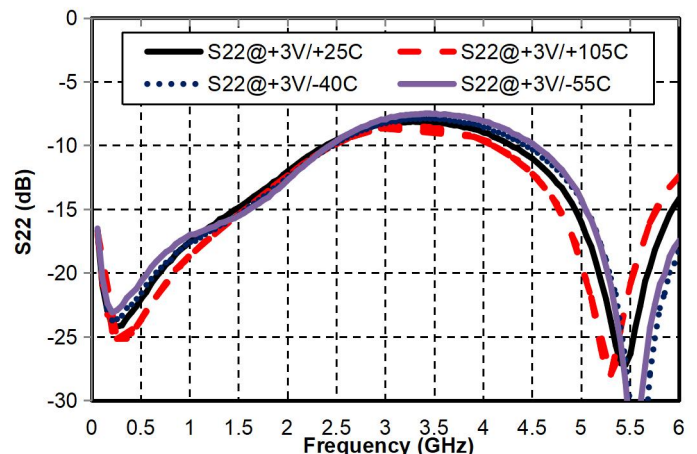
Noise Figure vs. Frequency



Input Return Loss vs. Frequency

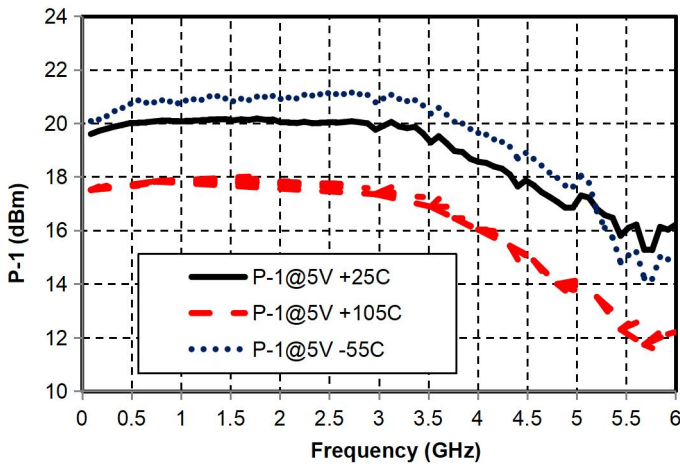


Output Return Loss vs. Frequency

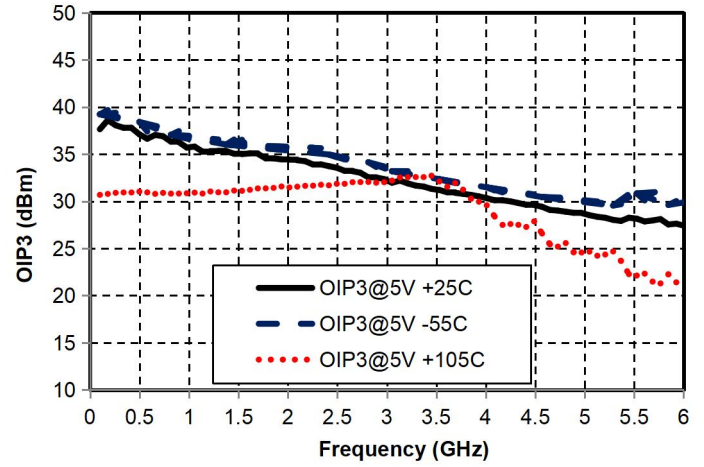


## High gain, high linearity, low noise gain amplifier , 50 - 6000 MHz

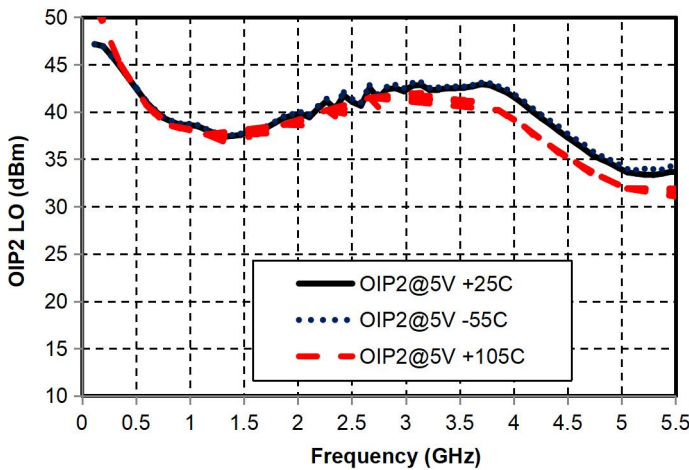
P-1dB vs. Frequency



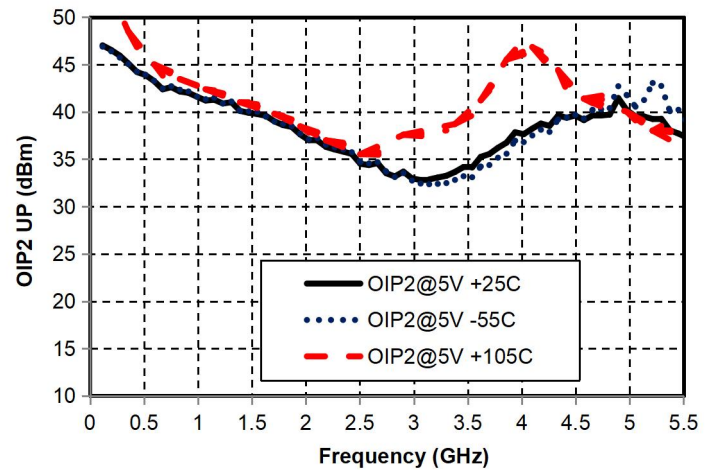
OIP3 vs. Frequency



OIP2 vs. Frequency (LOWER)



OIP2 vs. Frequency (UPPER)



## High gain, high linearity, gain amplifier , 50 - 6000 MHz

50M-6000M electrical performance parameters

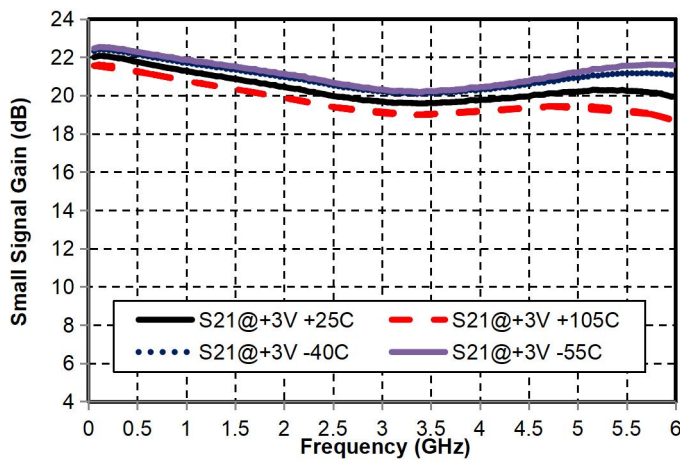
Electrical performance parameters ( TA = +25°C, VDD = +3V, 50Ω system , 55mA )

Index	Typical Value											Unit
	100	500	900	1200	1900	2300	3000	3600	4000	5000	6000	
Test frequency	100	500	900	1200	1900	2300	3000	3600	4000	5000	6000	MHz
Small Signal Gain	22.0	21.5	21.0	21.0	20.5	20.0	19.5	19.5	19.5	20.0	20.0	dB
Input return loss	13.0	14.0	14.0	13.0	11.0	9.0	8.5	10.0	11.5	10.0	5.0	dB
Output return loss	20.0	20.0	19.0	17.0	13.5	11.0	9.0	9.0	9.5	15.0	14.0	dB
P-1	14.0	15.5	16.0	16.0	16.0	16.0	15.0	14.5	13.5	12.0	11.0	dBm
OIP3	28.0	29.5	29.5	29.5	30.0	30.5	30.5	30.0	26.5	20.0	19.0	dBm
Noise Figure*	0.6	0.6	0.6	0.6	0.7	0.7	0.8	0.9	1.0	1.2	1.6	dB

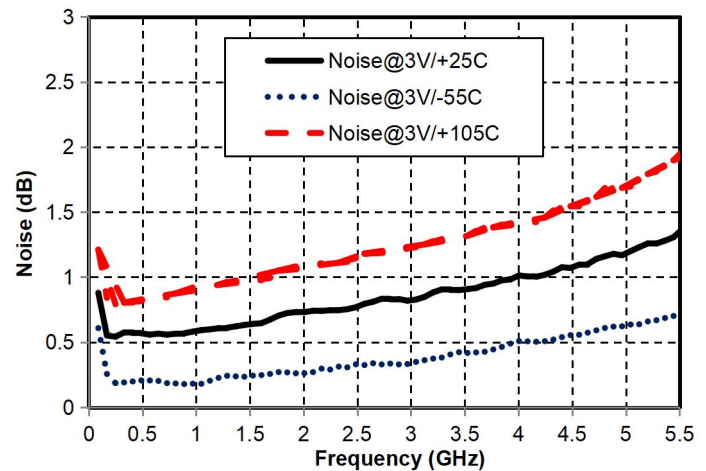
\*The noise figure result does not deduct the input loss of the test DEMO board .

Main index test curve ( TA = +25°C, VDD=+3V, 50Ω system)

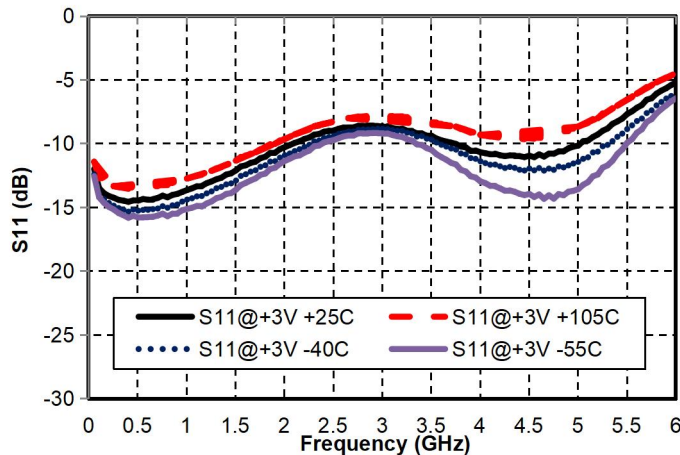
Small Signal Gain vs. Frequency



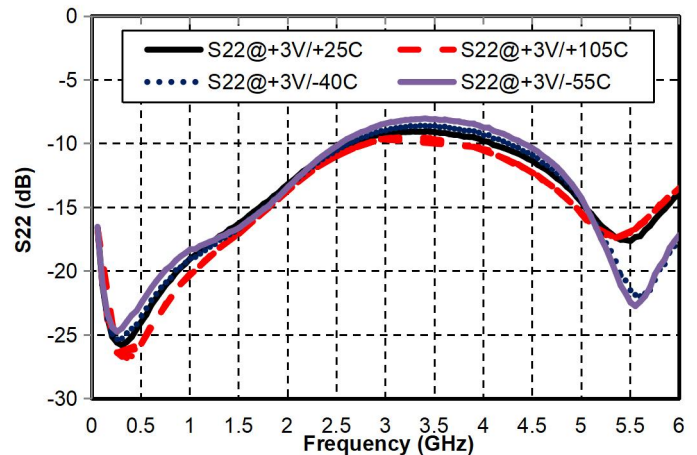
Noise Figure vs. Frequency



Input Return Loss vs. Frequency

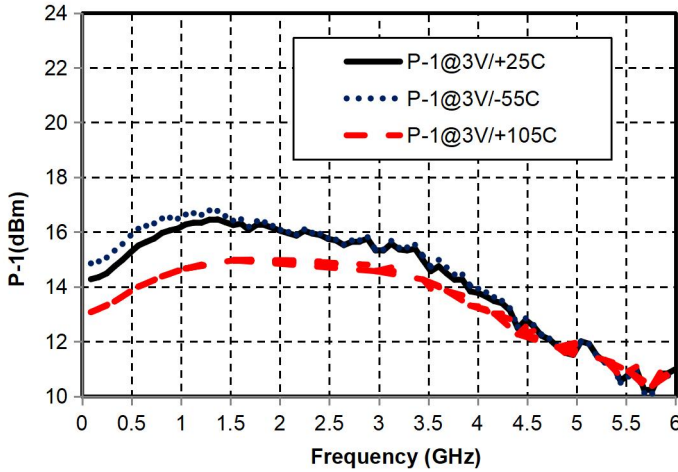


Output Return Loss vs. Frequency

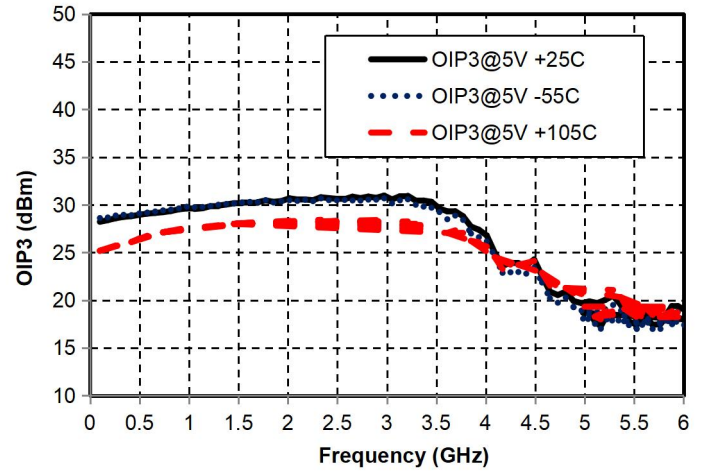


## High gain, high linearity, low noise gain amplifier , 50 - 6000 MHz

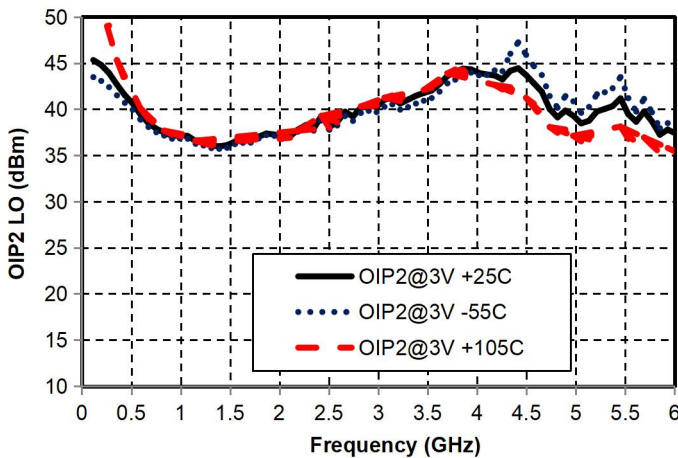
P-1dB vs. Frequency



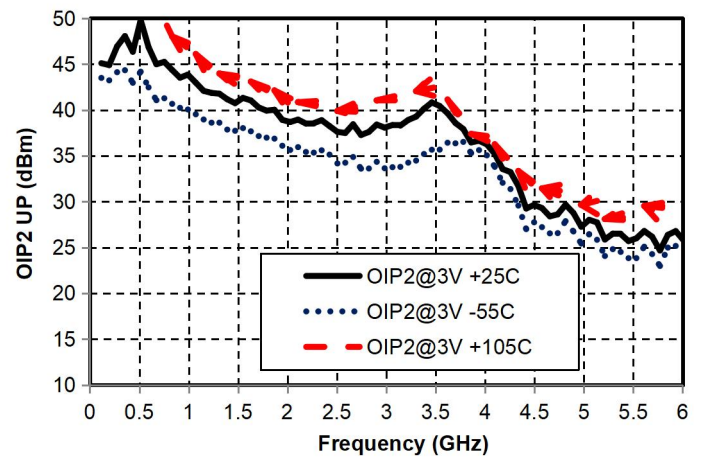
OIP3 vs. Frequency



OIP2 vs. Frequency (LOWER)



OIP2 vs. Frequency (UPPER)



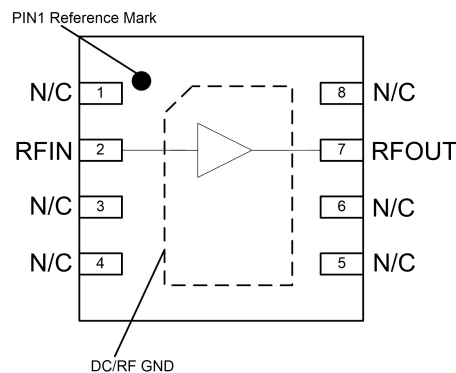
## High gain, high linearity, gain amplifier , 50 - 6000 MHz

### Bias resistor application

At a given bias voltage, the chip can tune the bias current (IDD) through pull-up or pull-down resistors . Please refer to the schematic on the previous page. The maximum IDD cannot exceed 120mA and the maximum junction temperature cannot exceed 150 °C. Note that in some cases, it may be necessary to re-optimize the return loss by adjusting L1 , L2 , C7 , and C6 .

IDD (mA)	3V		5V		6V		7V		8V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
95	48K	DNP	380K	DNP	DNP	80K	DNP	18.6K	DNP	8K
85	62K	DNP	DNP	DNP	DNP	38K	DNP	14.2K	DNP	6.8K
75	83K	DNP	DNP	90K	DNP	24K	DNP	11.3K	DNP	5.9K
65	120K	DNP	DNP	40K	DNP	17K	DNP	9.2K	DNP	5.1K
55	250K	DNP	DNP	25K	DNP	13K	DNP	7.6K	DNP	4.4K
45	DNP	DNP	DNP	17K	DNP	10K	DNP	6.3K	DNP	3.8K

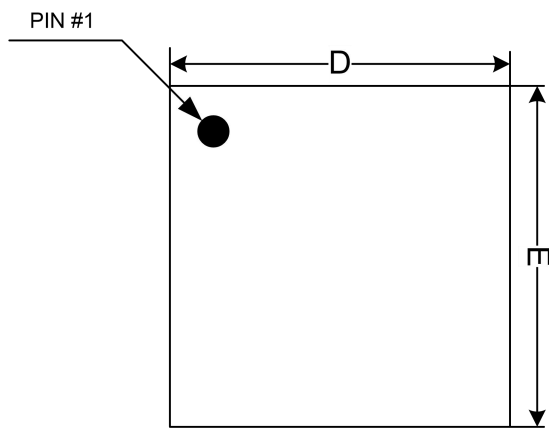
### Pin Definition



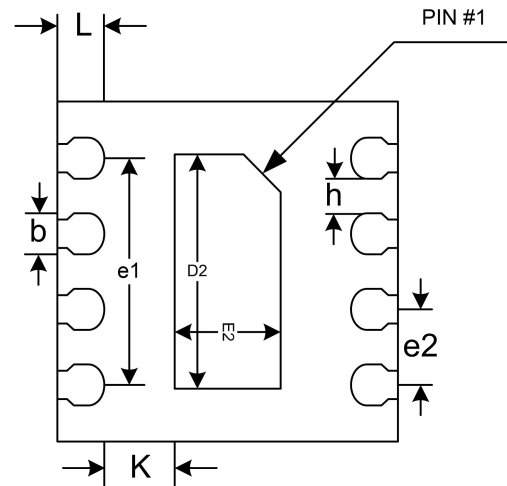
Bonding point number	Function Symbol	Functional Description
2	RF IN	RF input port, impedance 50ohm , requires external DC blocking capacitor
7	RF OUT / VDD	RF output port, impedance 50ohm, amplifier leakage bias, bias the circuit at the output end through external current-choking inductor and bias resistor, external DC blocking capacitor is required
1, 3, 4, 6, 8	GND	No connection required
5	VG2	Gate bias, no connection required
Chip bottom	GND	Grounding

## High gain, high linearity, gain amplifier , 50 - 6000 MHz

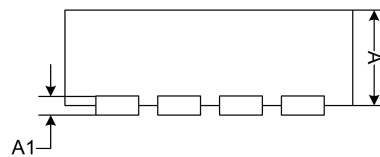
### Dimensions



Top view



Bottom view



Side View

### Structure size

Annotation	Minimum	Standard	Maximum	Annotation	Minimum	Standard	Maximum
A	0.70	0.75	0.80	E2	0.60	0.70	0.80
A1	0.10	0.12	0.15	e-1	1.40	1.50	1.60
b	0.20	0.25	0.30	e-2	0.40	0.50	0.60
D	1.90	2.00	2.10	h	0.10	0.20	0.30
D2	1.20	1.30	1.40	L	0.25	0.30	0.35
E	1.90	2.00	2.10	K	0.30	0.35	0.40

All units in the figures are millimeters .



## High gain, high linearity, gain amplifier , 50 - 6000 MHz

### Use limit parameters

Drain voltage: +10V	Input power: +20dBm
Maximum current: 120mA	Maximum junction temperature : 150 °C
Operating temperature: -55 ~ +125 ° C	Storage Temperature: -65 ~ +150°C
Exceeding any of these maximum limits may cause permanent damage.	

### Environmental conditions

parameter	grade	standard
ESD – Human Body Model (HBM)	1 B	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	C3	ESDA / JEDEC JS-001-2014
MSL – Moisture Sensitivity Level	MSL 3	IPC/JEDEC J-STD-020

### Precautions for use

- Plastic package material: Low-pressure injection molding plastic that meets ROHS specifications
- Lead frame material: Nickel alloy
- Lead surface plating: 100% matte tin
- Maximum reflow peak temperature: 260 °C