

## GaAs MMIC 6-bit CNC Attenuator Chip, 0.1-12GHz

### Performance characteristics

Frequency range: 0.1-12GHz  
 Insertion loss: 2.7dB@12GHz  
 Attenuation range: 0.5~31.5dB  
 Bit count: 6  
 Attenuation accuracy (RMS): 0.4dB  
 50Ohm input/output  
 Chip size: 1.50 x 1.0 x 0.1mm

### Product Introduction

GDA-0012-6I-PD is a GaAs MMIC 6-bit CNC attenuator chip, with a frequency range of 0.1-12GHz, insertion loss of 2.0dB, switching speed of 25ns, integrated driver inside the chip, using +5V power supply and 0/+5V control (compatible with +3.3V).

### Usage restriction parameter 1

Power supply voltage range	+6V
Control voltage range	-0.5V~+5.5V
Maximum input power	+27dBm
Working temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of the above maximum limits may result in permanent damage.

### Electrical performance parameters(Ta=+25°C, VDD=+5V, 0/+5V Control)

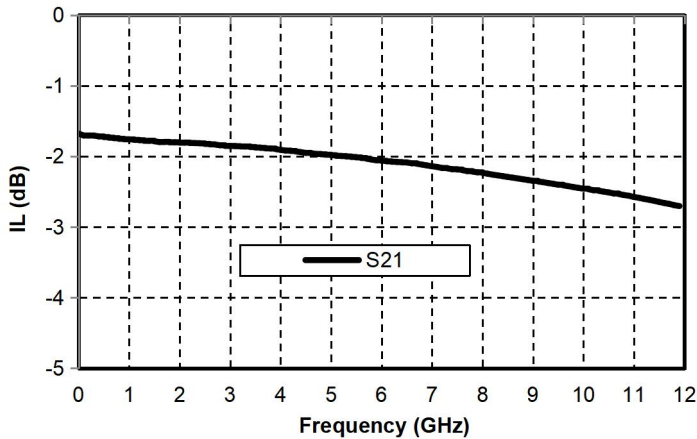
Index	Minimum value	Typical value	Maximum value	Unit
Frequency range	0.1~12			GHz
Insertion loss	-	2.2	-	dB
Attenuation range	0.5~31.5			dB
Attenuation step	0.5			dB
Attenuation number	6			bits
Attenuation accuracy (all frequency bands)	-	±1.5	-	dB
Attenuation accuracy RMS	-	0.4	-	dB
Additional phase shift	-	±7	-	degree
Additional phase shift RMS	-	2.0	-	
Input return loss	-	20	-	dB
Output Return Loss	-	20	-	dB
Switching speed	-	25	-	ns
P-1dB	-	23	-	dBm

supply voltage	+3	+5	-	V
Power supply current	-	8		mA
Control high level	+2.5	+3.3	+5	V
Control low level	0	-	0.8	V
Control current	-	-	1	mA

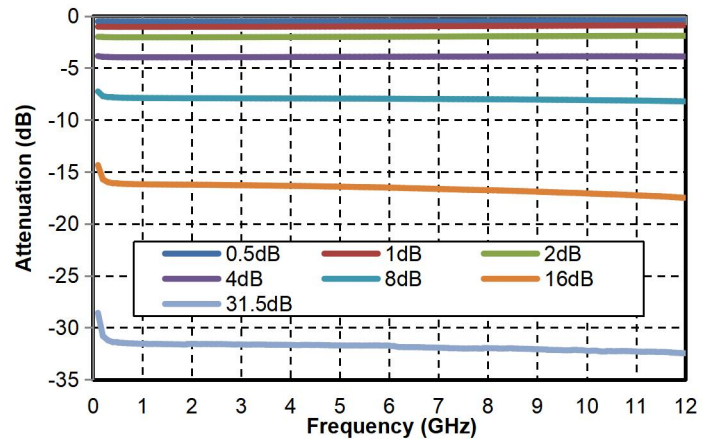
## GaAs MMIC 6-bit CNC Attenuator Chip, 0.1-12GHz

Main indicator testing curve

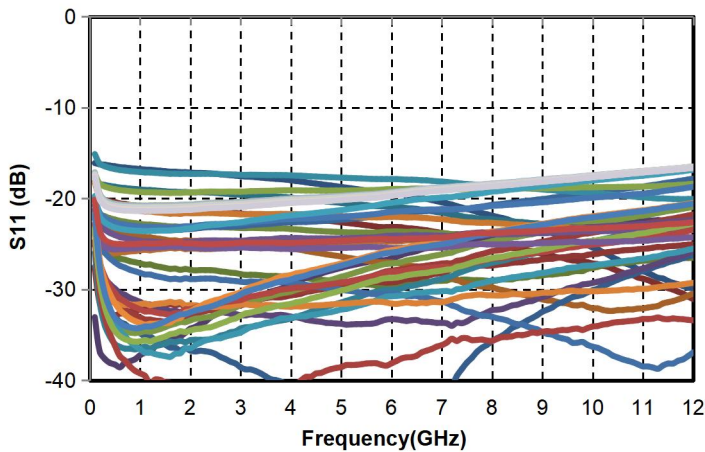
Insertion loss vs. Frequency



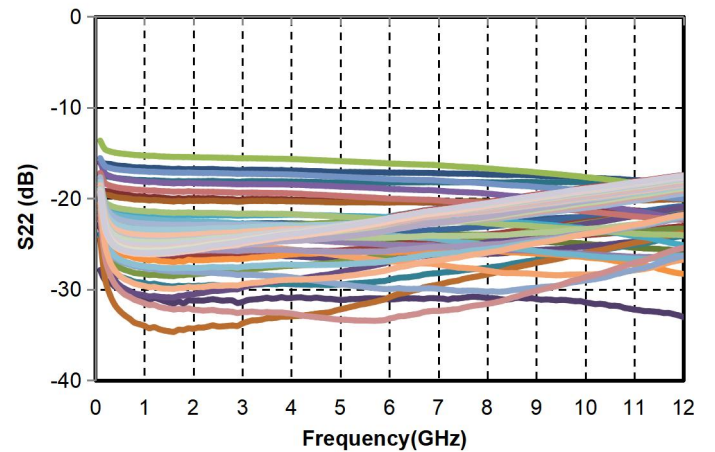
Reference Decay State vs. Frequency



Input return loss vs. Frequency

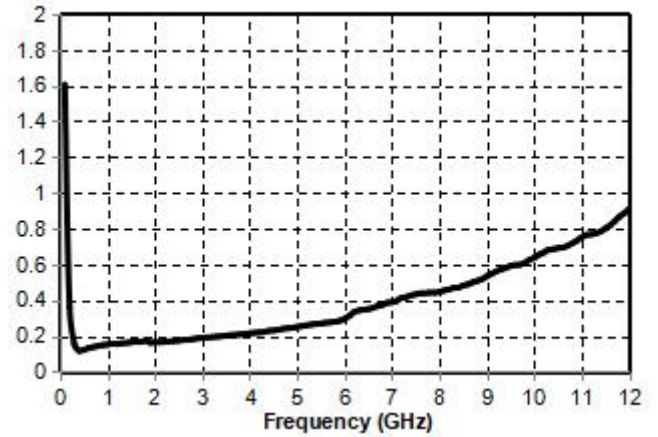
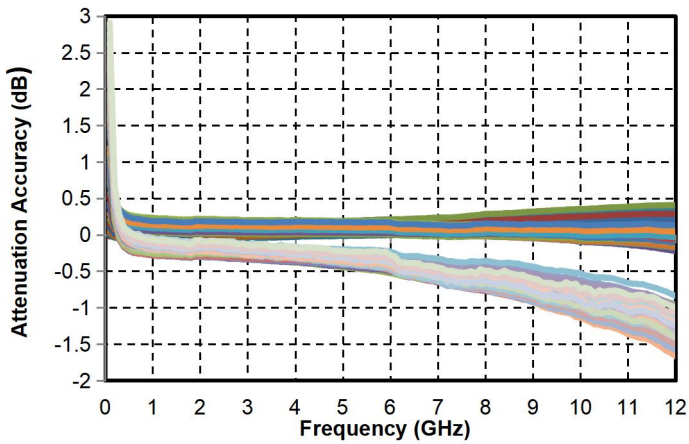


Output return Loss vs. Frequency



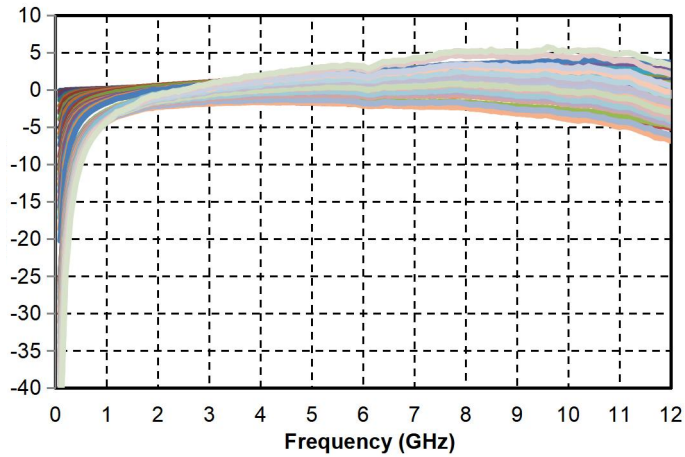
Attenuation Accuracy vs. Frequency

Attenuation Accuracy RMS vs. Frequency

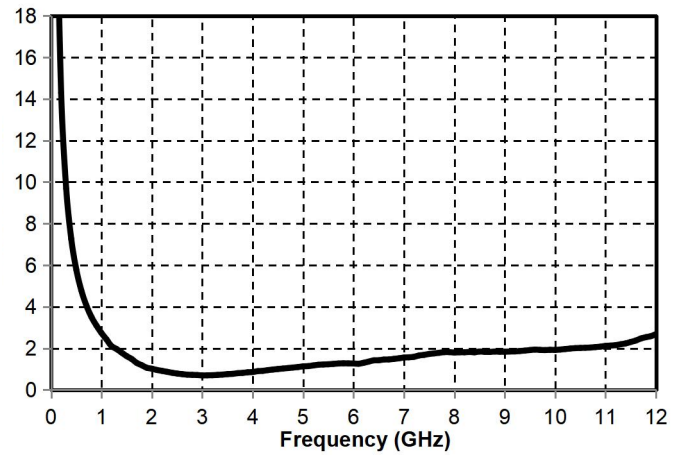


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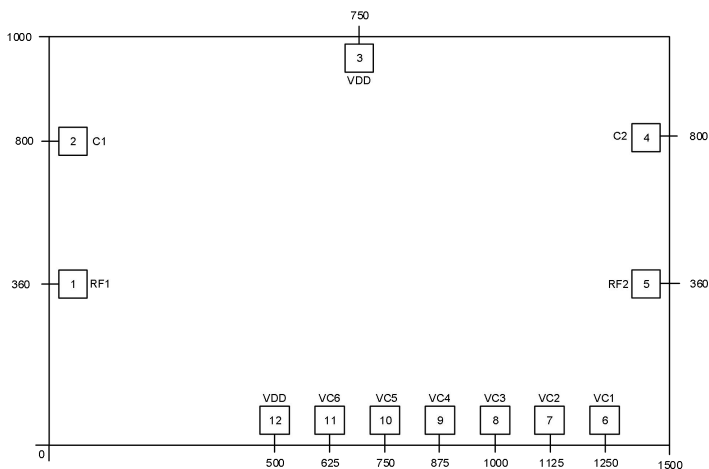
Additional Phase Shift vs. Frequency



Additional Phase Shift RMS vs. Frequency



### External Structure 2



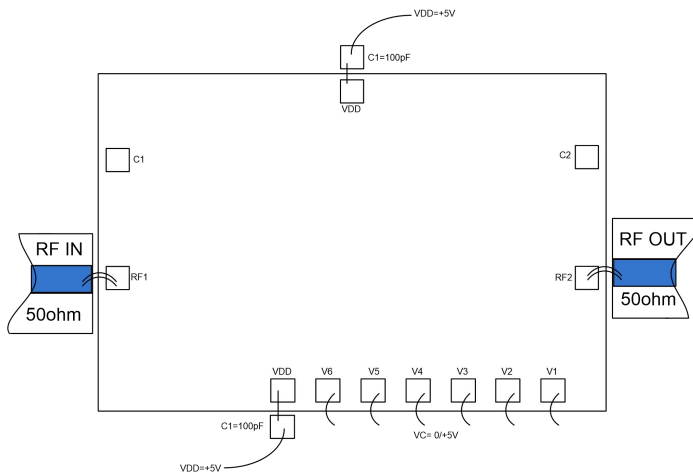
[2] The units in the figure are all micrometers, and the tolerance for external dimensions is  $\pm 50\mu\text{m}$ .

Definition of bonding pressure point		
Bond point number	Functional symbols	Function Description
1	RF1	The signal input terminal is externally connected to a 50 ohm circuit and requires an additional broadband DC isolation capacitor.
5	RF2	The signal output terminal is externally connected to a 50 ohm circuit and requires an additional broadband DC isolation capacitor.
3、 12	VDD	The chip power port requires an external 100pF capacitor (one can be selected).
6~11	VC	Attenuation control pads, refer to the truth table for attenuation control.
2、 4	C1, C2	Can be externally connected with capacitors to improve low-frequency characteristics.
Chip bottom	GND	The bottom of the chip needs to have sufficient and good contact with RF and DC ground.

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Truth table							
VDD	VC1	VC2	VC3	VC4	VC5	VC6	Conduction pathway
+5V	+5V	+5V	+5V	+5V	+5V	+5V	Initial state N=0: attenuation amount is 0
	+5V	+5V	+5V	+5V	+5V	0V	Attenuation state N=1: Attenuation amount is 0.5
	+5V	+5V	+5V	+5V	0V	+5V	Attenuation state N=2: Attenuation amount is 1
	+5V	+5V	+5V	0V	+5V	+5V	Attenuation state N=4: Attenuation amount is 2
	+5V	+5V	0V	+5V	+5V	+5V	Attenuation state N=8: Attenuation amount is 4
	+5V	0	+5V	+5V	+5V	+5V	Attenuation state N=16: Attenuation amount is 8
	0V	+5V	+5V	+5V	+5V	+5V	Attenuation state N=32: Attenuation amount is 16
	0V	0V	0V	0V	0V	0V	Attenuation state N=63: attenuation amount is 31.5

## Recommended assembly diagram



Connect the VDD on one side and control the solder pads without the need for external resistors.

## Notice

- The chip needs to be stored in a container with anti-static function and stored in a nitrogen environment.
- Attempting to clean the surface of bare chips using wet chemical methods is prohibited.
- Please strictly comply with ESD protection requirements to avoid static damage to bare chips.
- Routine operation: Please use precision pointed tweezers to remove the bare chip. During the operation, avoid tools or fingers touching the surface of the chip.
- Suggestion for mounting operation: Bare chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold tin ratio of 80/20. The working surface temperature reached 255 °C, and the tool (vacuum chuck) temperature reached 265 °C. When a high-temperature mixed gas (nitrogen to hydrogen ratio of 90/10) is blown onto the chip, the temperature at the top of the tool should be raised to 290 °C. Do not let the chip stay above 320 °C for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive adhesive applied should be as small as possible. After placing the chip in the installation position, the conductive adhesive can be vaguely visible around it. Please follow the information provided by the conductive adhesive manufacturer for curing conditions.
- Suggestion for bonding operation: Both spherical or wedge-shaped bonding should be made of gold wire with a diameter of 0.025mm (1mil). Thermal ultrasonic bonding temperature is 150 °C. The pressure of the spherical bonding cutter is 40-50GF, and the pressure of the wedge bonding cutter is 18-22GF. Use as little ultrasonic energy as possible. The bonding process starts at the pressing point on the chip and ends at the packaging (or substrate).