GDA-0008-6D-P-PD

GaAs MMIC 6-bit Digital Attenuator Chip, 0.5-8GHz

Performance characteristics

Frequency range: 0.5-8GHz
Insertion loss: 3.0dB@8GHz
Attenuation range: 0.5~31.5dB
Bit Count: 6 digits
Attenuation accuracy (RMS): 0.15dB
50Ohm input/output
Chip size: 1.65 x 1.1 x 0.1mm

Product Introduction

GDA-0008-6D-P-PD is a GaAs MMIC 6-bit Digital Attenuator Chip, with a frequency range of 0.5-8GHz, insertion loss of 3dB, switching speed of 30ns, and integrated driver inside the chip. It adopts+5V power supply and 0/+5V control (compatible with+3.3V).

Usage restriction parameter[1]	
Power supply voltage range	+6V
Control voltage range	-0.5V~+5.5V
Maximum input power	+27dBm
working temperature	-55 ~ +85°C
Storage temperature	-65 ~ +150°C

【1】 Exceeding any of the above maximum limits may result in permanent damage.

Electrical parameters(Ta=+25°C，VEE=+5V，0/+5V Control)				
Index	Minimum value	Typical value	Maximum value	Unit
Frequency range	0.5~8			GHz
Insertion loss @ 8GHz	-	3.0	-	dB
Attenuation range	0.5~31.5			dB
Attenuation step	0.5			dB
Attenuation number	6			bite
Attenuation accuracy (all frequency bands)	-	±0.2	-	dB
Attenuation accuracy RMS	-	0.15	-	dB
Additional phase shift	-	±3	-	degree
Additional phase shift RMS	-	1.5	-	degree
Input return loss	-	20	-	dB
Output Return Loss	-	20	-	dB
Switching speed	-	30	-	ns
P-1dB@1-8GHz	-	21	-	dBm
Supply voltage	-	+5	-	V

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Power supply current	-	9		mA
Control high level	+2.7	+3.3	+5	V
Control low level	0	-	0.8	V
Control current	-	1	-	mA

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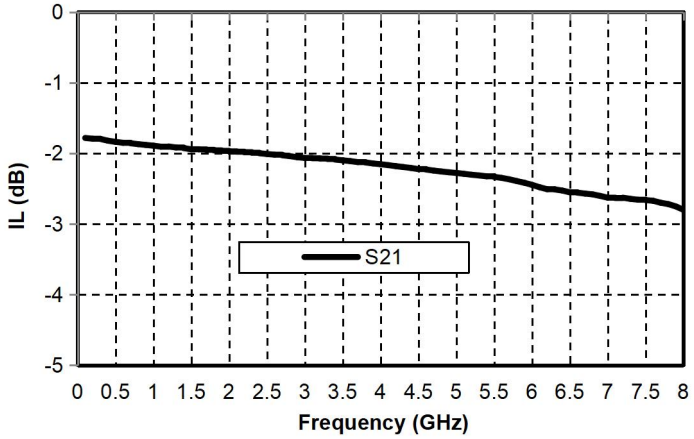
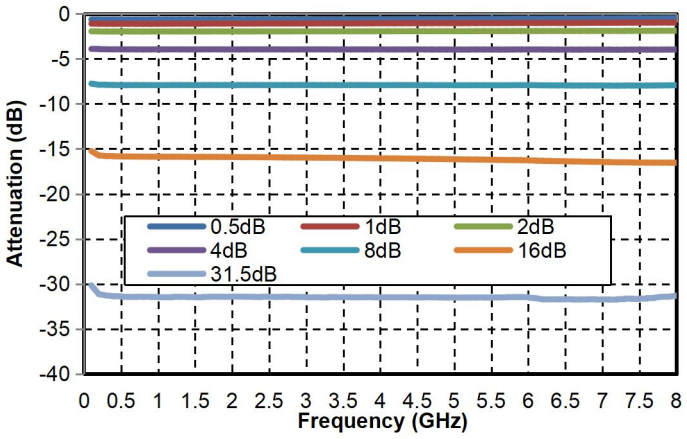
Main indicator testing curve

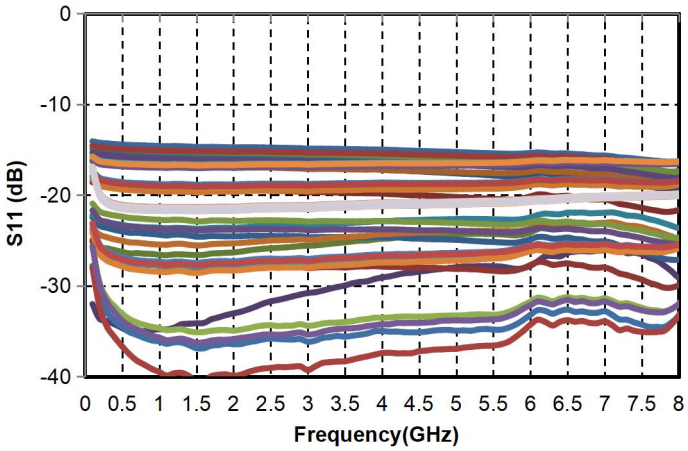
Insertion loss vs. Frequency



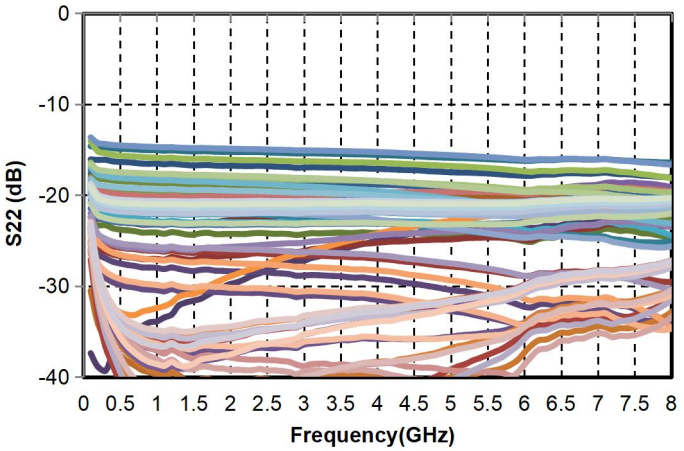
Reference attenuation state vs. Frequency



Input echo vs. Frequency

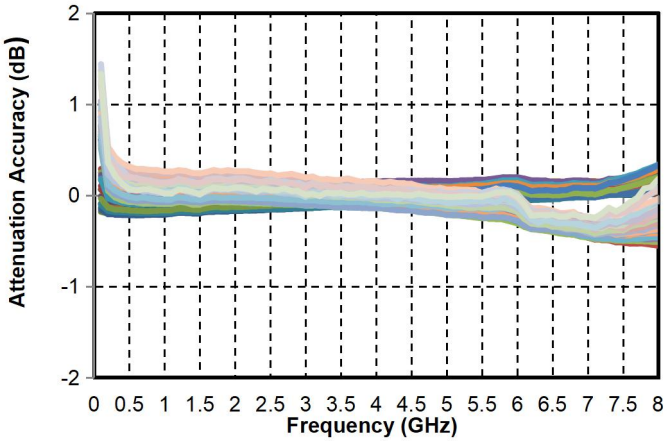


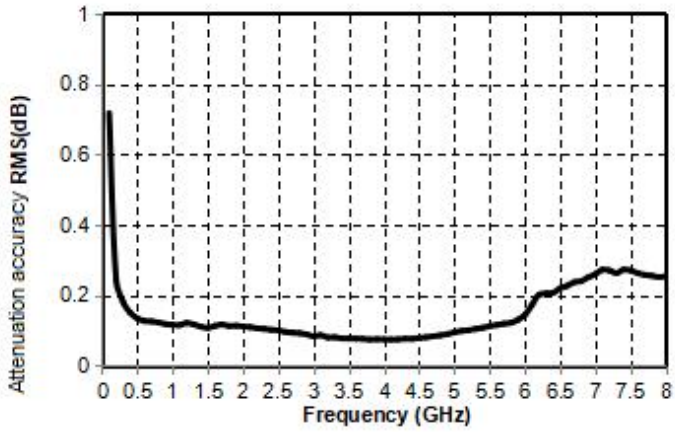
Output echo vs. Frequency



Attenuation accuracy vs. Frequency

Attenuation accuracy RMS vs. Frequency





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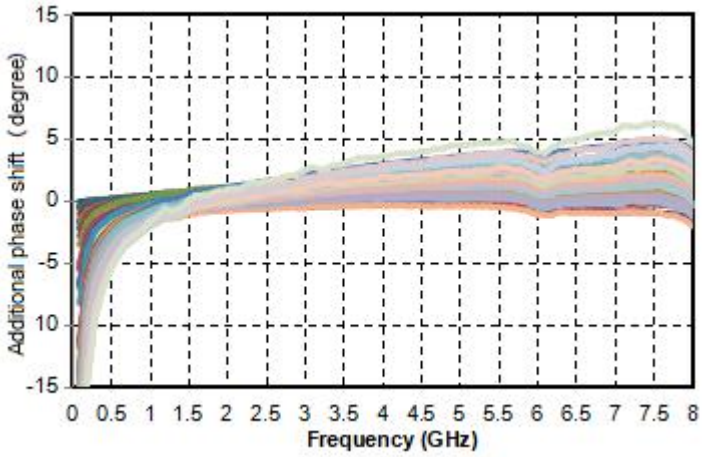
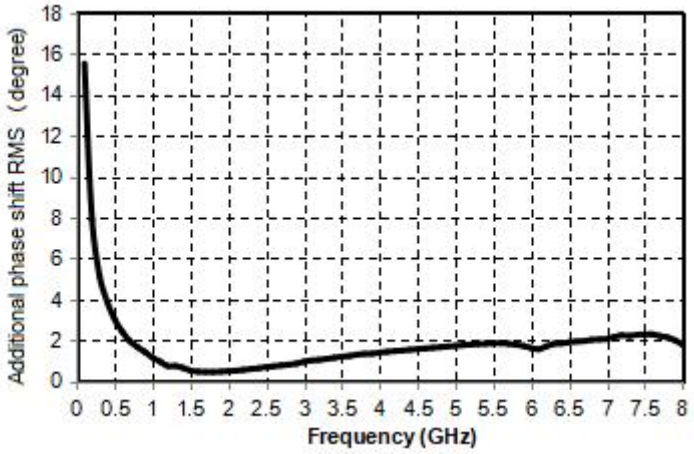
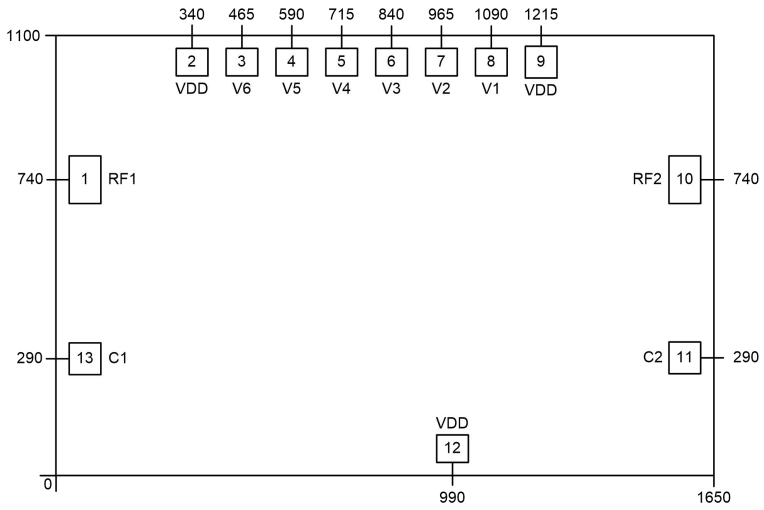
Additional phase shift vs. Frequency



Additional phase shift RMS vs.Frequency



External structure[2]



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[2] The units in the figure are all micrometers. (Boundary dimension tolerance: ±50um.)

Definition of bonding pressure point		
Bond point number	Functional symbols	Function Description
1	RF1	The signal input terminal is externally connected to a 50 ohm circuit, and there is no integrated DC isolation capacitor inside the chip
5	RF2	The signal output terminal is externally connected to a 50 ohm circuit, and there is no integrated DC isolation capacitor inside the chip
3、12	VDD	The chip power port requires an external 100pF capacitor (one can be selected)
6~11	VC	Attenuation control pads, refer to the truth table for attenuation control
2、4	C1，C2	Can be externally connected with capacitors to improve low-frequency characteristics
Chip bottom	GND	The bottom of the chip needs to have sufficient and good contact with RF and DC ground

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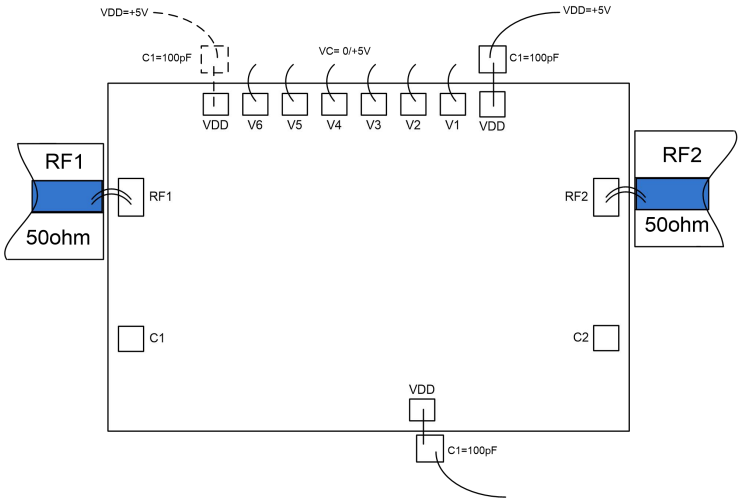
Truth table							
VC1	VC2	VC3	VC4	VC5	VC6	VDD	Conduction pathway
High（1）	High（1）	High（1）	High（1）	High（1）	High（1）	+5V	Initial state N=0: attenuation amount is 0
High（1）	High（1）	High（1）	High（1）	High（1）	Low（0）		Attenuation state N=1: Attenuation amount is 0.5
High（1）	High（1）	High（1）	High（1）	Low（0）	High（1）		Attenuation state N=2: Attenuation amount is 1
High（1）	High（1）	High（1）	Low（0）	High（1）	High（1）		Attenuation state N=4: Attenuation amount is 2
High（1）	High（1）	Low（0）	High（1）	High（1）	High（1）		Attenuation state N=8: Attenuation amount is 4
High（1）	Low（0）	High（1）	High（1）	High（1）	High（1）		Attenuation state N=16: Attenuation amount is 8
Low（0）	High（1）	High（1）	High（1）	High（1）	High（1）		Attenuation state N=32: Attenuation amount is 16
Low（0）	Low（0）	Low（0）	Low（0）	Low（0）	Low（0）		Attenuation state N=63: attenuation amount is 31.5

High（1），+2.7~+5V；Low（0），0~+0.8V

Suggested assembly diagram（Connect the VEE on one side and control the solder pads without the need for external resistors.）



Precautions for use

- The chip needs to be stored in a container with anti-static function and stored in a nitrogen environment.
- Attempting to clean the surface of bare chips using wet chemical methods is prohibited.
- Please strictly comply with ESD protection requirements to avoid static damage to bare chips.
- Routine operation: Please use precision pointed tweezers to remove the bare chip. During the operation, avoid tools or fingers touching the surface of the chip.
- Suggestion for mounting operation: Bare chip installation can use AuSn solder eutectic sintering or conductive adhesive bonding process. The installation surface must be clean and flat.
- Sintering process: It is recommended to use AuSn solder sheets with a gold tin ratio of 80/20. The working surface temperature reached 255 ℃, and the tool (vacuum chuck) temperature reached 265 ℃. When a high-temperature mixed gas (nitrogen to hydrogen ratio of 90/10) is blown onto the chip, the temperature at the top of the tool should be raised to 290 ℃. Do not let the chip stay above 320 ℃ for more than 20 seconds. The friction time should not exceed 3 seconds.
- Bonding process: The amount of conductive adhesive applied should be as small as possible. After placing the chip in the installation position, the conductive adhesive can be vaguely visible around it. Please follow the information provided by the conductive adhesive manufacturer for curing conditions.
- Suggestion for bonding operation: Both spherical or wedge-shaped bonding should be used Φ 0.025mm (1mil) gold wire. Thermal ultrasonic bonding temperature is 150 ℃. The pressure of the spherical bonding cutter is 40-50GF, and the pressure of the wedge bonding cutter is 18-22GF. Use as little ultrasonic energy as possible. The bonding process starts at the pressing point on the chip and ends at the packaging (or substrate).